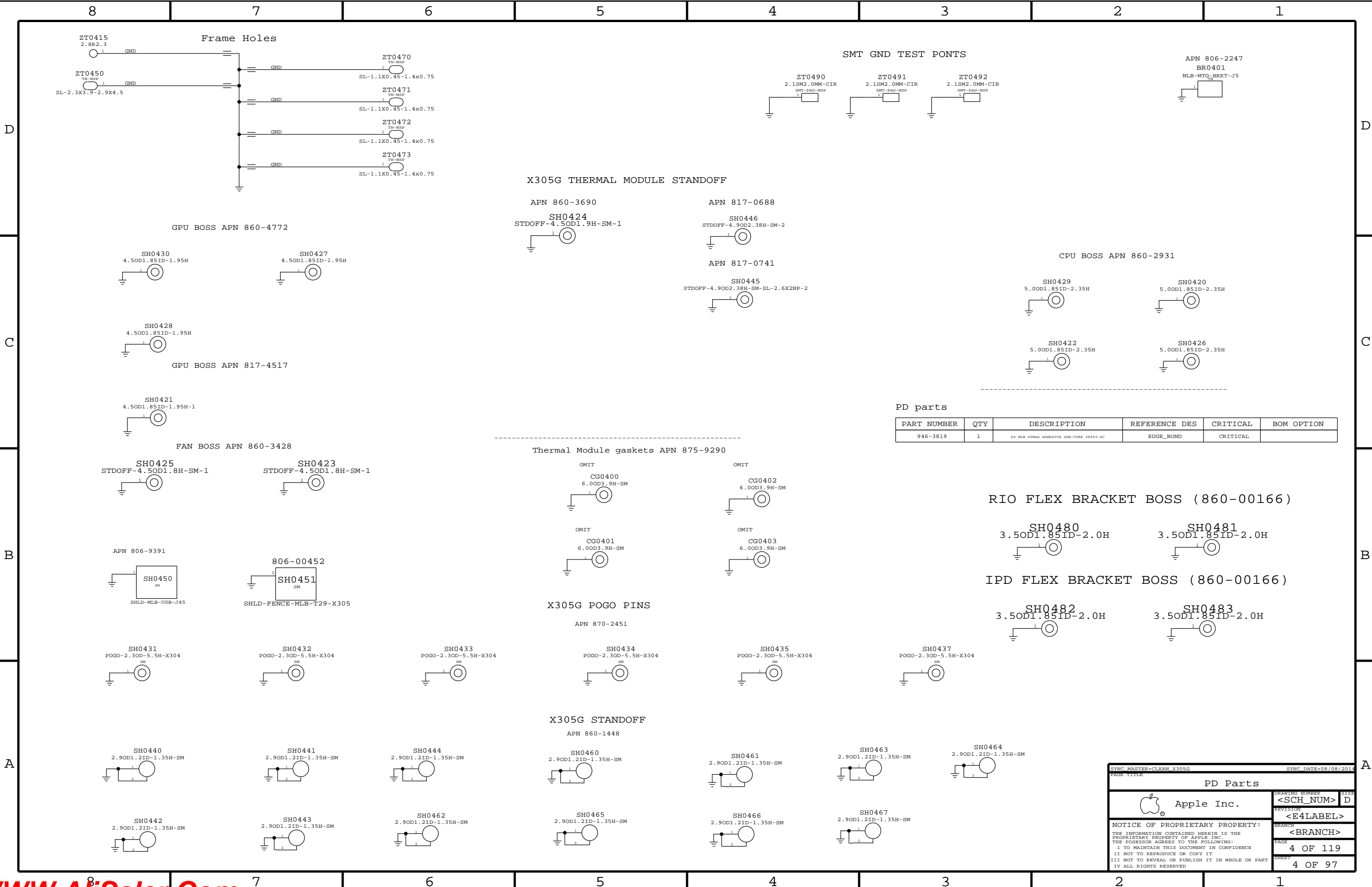



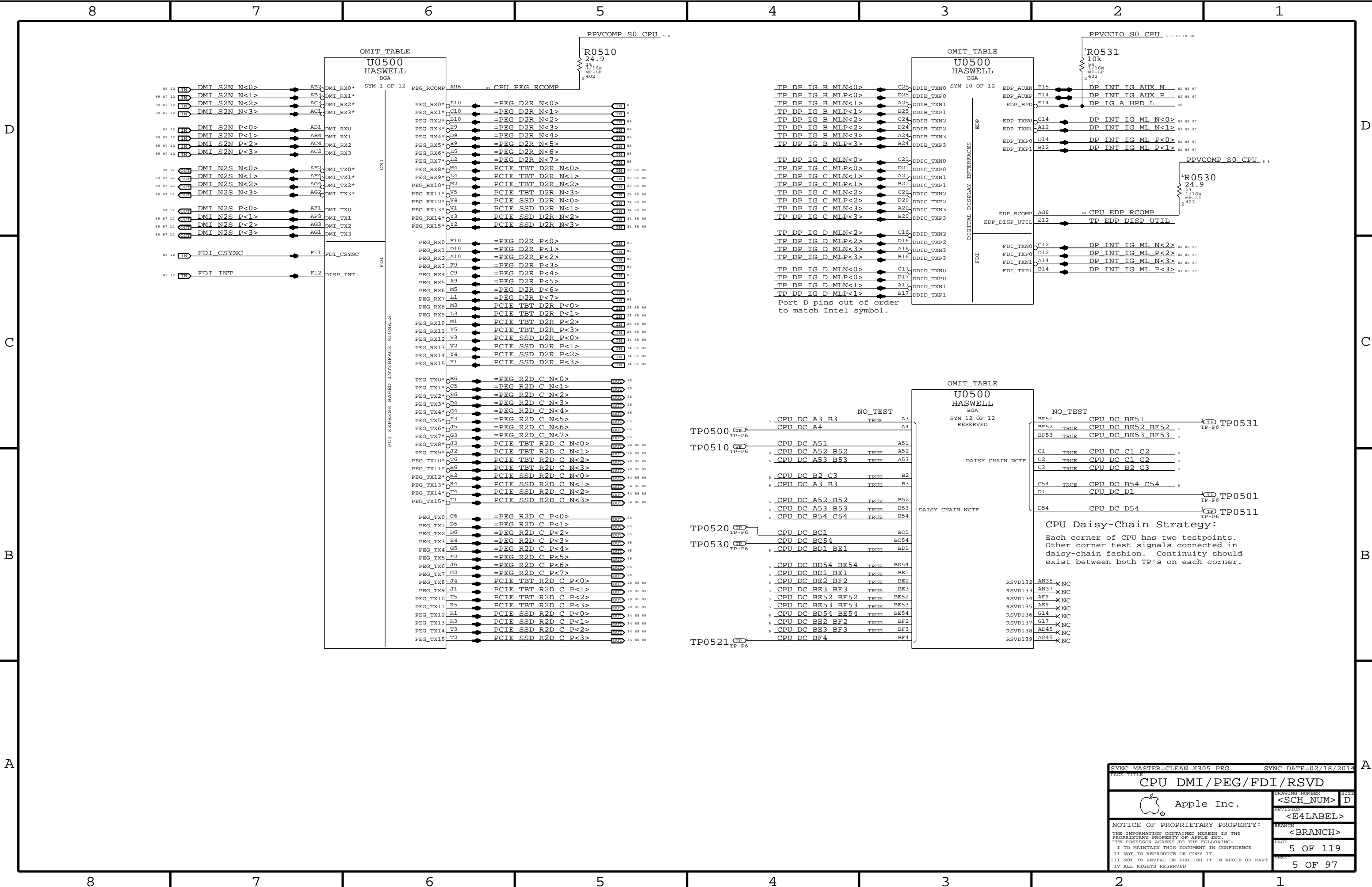
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Programmables - All builds							
335S0915	1	IC,SERIAL SPI FLASH ROM,4MBIT,50MHZ,USON	U2890	CRITICAL	TBTROM:BLANK		
341S00166	1	T29,FALCON RIDGE(V27.1)PROTO0,X425G	U2890	CRITICAL	TBTROM:PROG		
335S0724	1	1MBIT SERIAL FLASH 2KX0.6MM UFDFPN8 PKG	U9101	CRITICAL	GPUROM:BLANK		
341S3565	1	IC,EDP MUX-95C,(RENESAS) V3.2.8,DVB,D2	U9600	CRITICAL	DPMUXMCU:PROG		
337S4313	1	IC,MCU,H8S/2113,9X9MM,TLP-145V	U9600	CRITICAL	DPMUXMCU:BLANK		
SMC							
338S1214	1	IC,SMC-B1,40MHZ/50DMIPS,SCPL FW,157BGA	U5000	CRITICAL	SMC_PROG:BLANK		
341S00157	1	IC,SMC-B1,EXT (V2.25A9) PROTO 0,X425G	U5000	CRITICAL	SMC_PROG:BASE		
EFI ROM							
335S00007	1	IC,SERIAL FLASH,64MB,3V,WS0N,6X5MM	U6100	CRITICAL	BOOTROM_BLANK:WIN		
335S00006	1	IC,SERIAL FLASH,64MB,3V,WS0N,6X5MM	U6100	CRITICAL	BOOTROM_BLANK:MAC		
341S00239	1	IC,EFI ROM (V0145) EVT,X425	U6100	CRITICAL	BOOTROM_PROG:EVT		
Alternate Parts							
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:			
376S1053	376S0604		ALL	Diodes alt to Fairchild			
128S0311	128S0329		ALL	NEC alt to Sanyo			
138S0739	138S0706		ALL	Samsung alt to Murata			
197S0481	197S0480		ALL	Spsom Alt to NDK			
197S0478	197S0479		ALL	NDK Alt to Spsom			
371S0713	371S0558		ALL	DDG alt to ST			
152S0461	152S1645		ALL	Cyntec alt to Vishay			
376S1080	376S0820		ALL	Diodes alt to On Semi			
155S0667	155S00008		ALL	Panasonic alt to TDK			
376S00074	376S0855		ALL	Toshiba alt to Diodes			
376S1129	376S0855		ALL	NXP alt to Diodes			
376S1089	376S1128		ALL	NXP alt to Diodes			
128S0371	128S0376		ALL	Kemet alt to Sanyo			
138S0803	138S0639		ALL	Samsung alt to Murata			
138S0843	138S0674		ALL	Samsung alt to Murata			
138S0846	138S0811		ALL	Samsung alt to Murata			
127S0164	127S0162		ALL	Rohm alt to Vishay			
138S0732	138S0715		ALL	Rohm alt to Vishay			
128S0364	128S0264		ALL	Kemet alt to Sanyo			
333S0704	333S0700		ALL	ELPIDA to HYNIX U4000			
311S0649	311S0541		ALL	ON alt to Toshiba			
376S00014	376S0761		ALL	Toshiba alt to Vishay			
740S00003	740S0135		ALL	ARM alt to Tyco			
740S00004	740S0134		ALL	ARM alt to Littelfuse			
107S00029	107S00030		ALL	TFT alt to Cyntec			
128S0398	128S0220		ALL	Kemet alt to Sanyo			
128S0386	128S0284		ALL	Kemet alt to Sanyo			
311S00008	311S0271		ALL	Diodes alt to NXP			
128S0393	128S0334		ALL	Kemet alt to Sanyo			
311S00007	311S0426		ALL	Diodes alt to NXP			
371S00017	371S0749		ALL	Diodes alt to Onsemi			
107S00033	107S00034		ALL	TFT alt to Cyntec			
107S0240	107S0255		ALL	TFT alt to Cyntec			
107S0248	107S0250		ALL	TFT alt to Cyntec			
107S00031	107S00032		ALL	TFT alt to Cyntec			
107S0249	107S0251		ALL	TFT alt to Cyntec			
107S00037	107S00038		ALL	TFT alt to Cyntec			
107S00015	107S00011		ALL	TFT alt to Cyntec			
128S00008	128S0380		ALL	NEC alt to Sanyo			
311S00060	311S0273		ALL	Diodes alt to NXP			
353S00133	353S2741		ALL	ON Semi alt to TI			
353S00394	353S2162		ALL	ON Semi alt to TI			
376S00086	376S0761		ALL	Diodes alt to Vishay			
112S00001	112S0254		ALL	Yageo alt to Cyntec			</

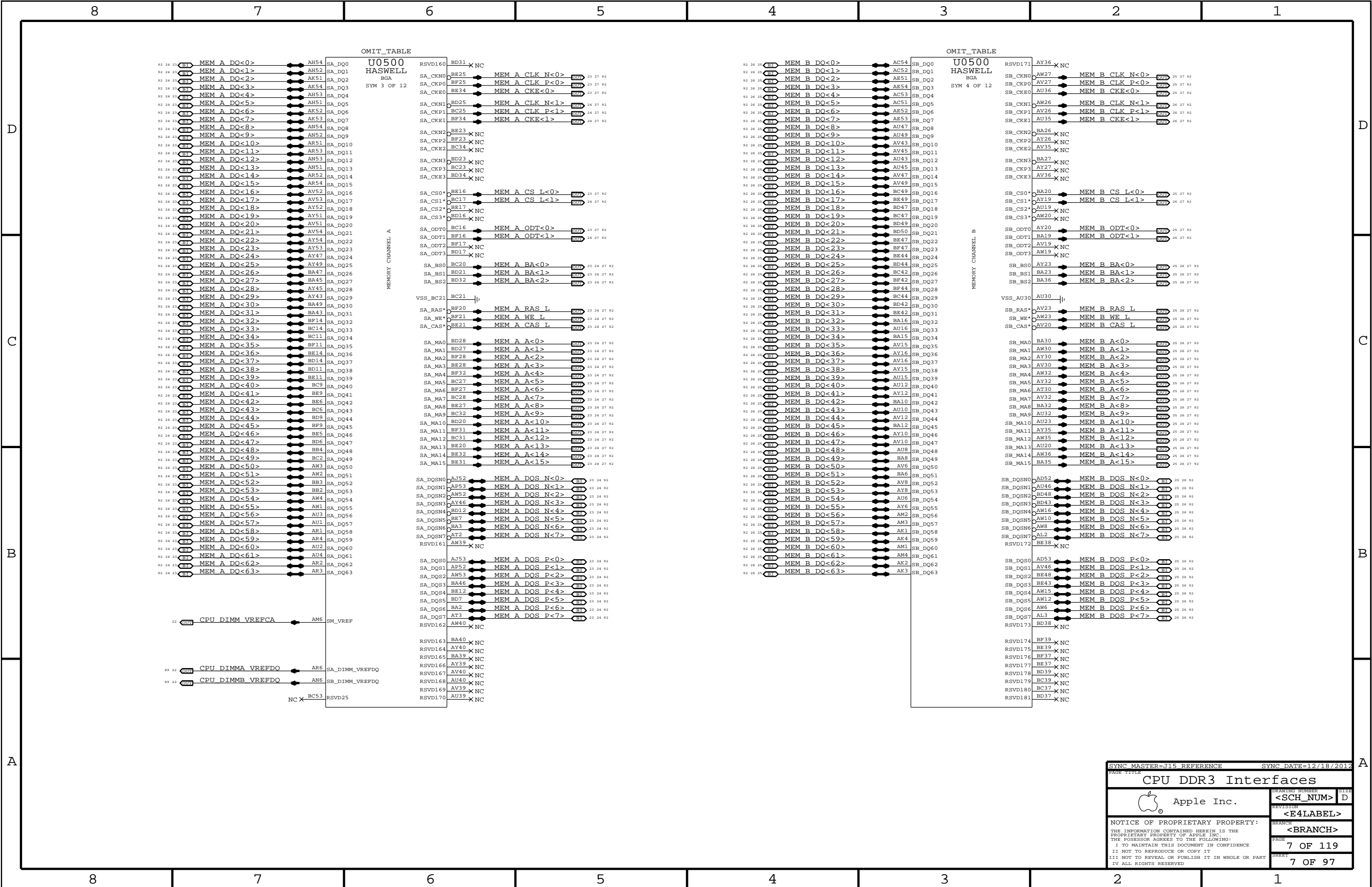


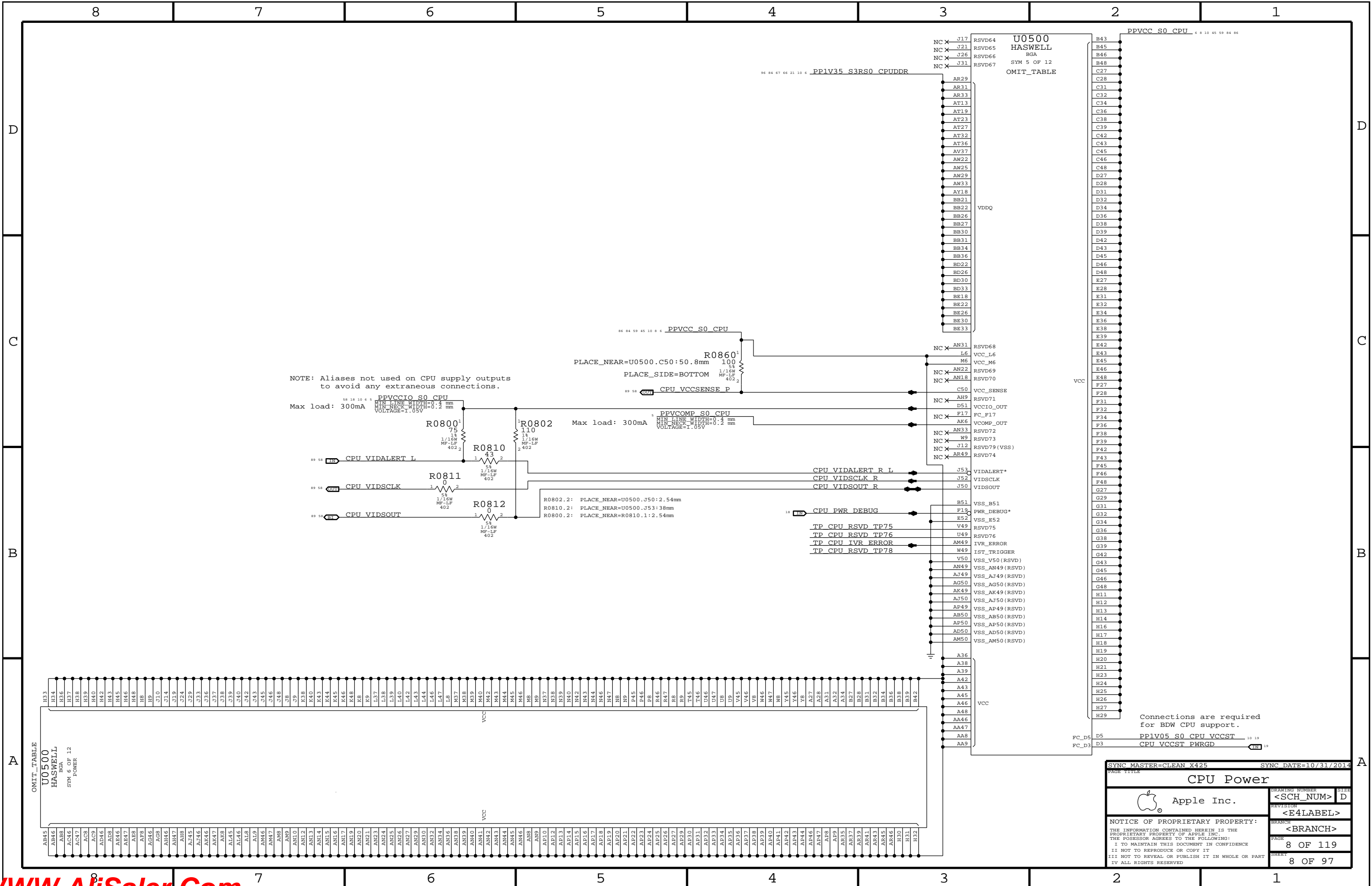
PD parts

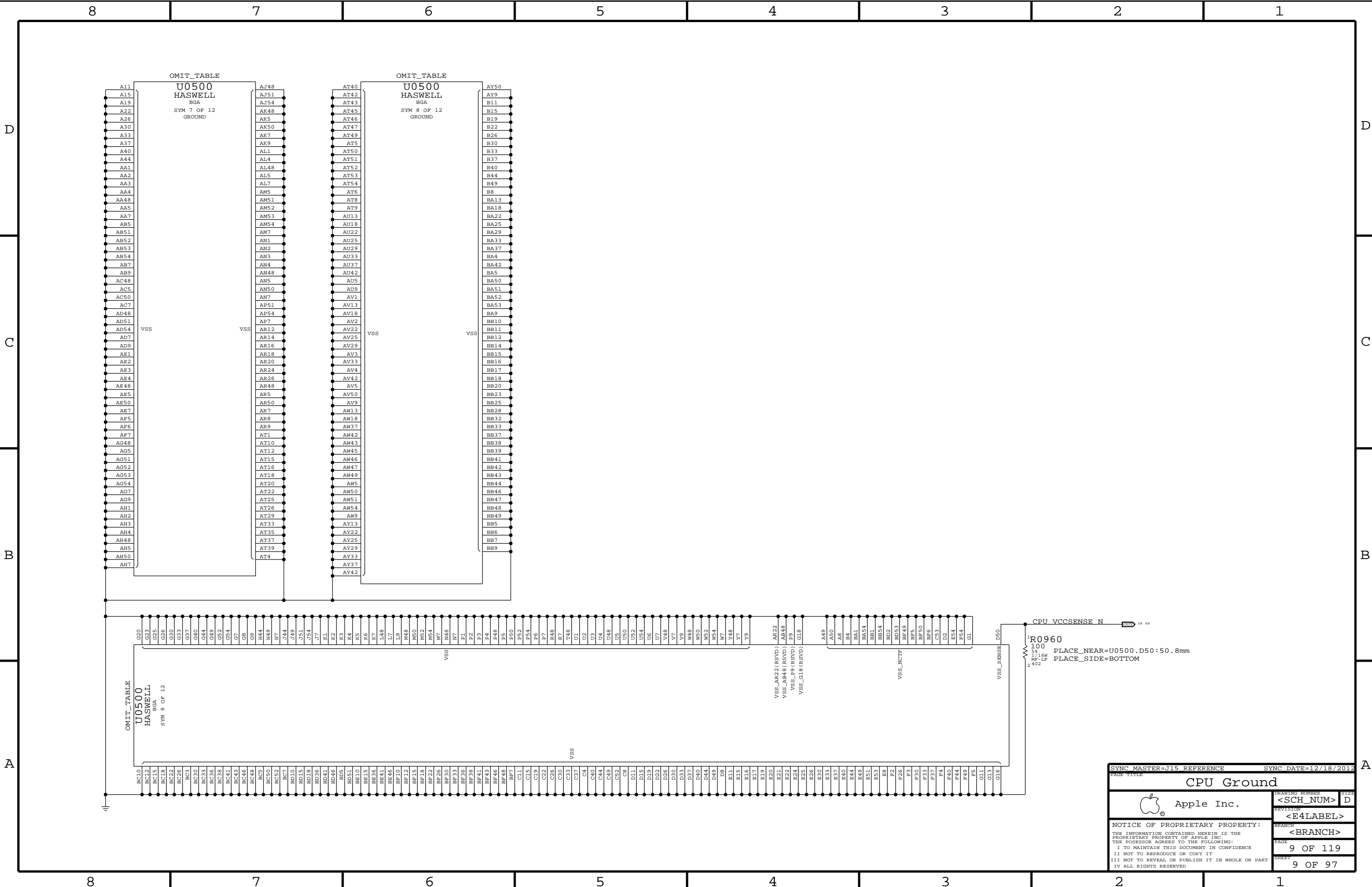
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
946-3819	1	D2 MLB DYMAX ADHESIVE DES-CURR 29993-0C	EDGE_BOND	CRITICAL	


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PD Parts			
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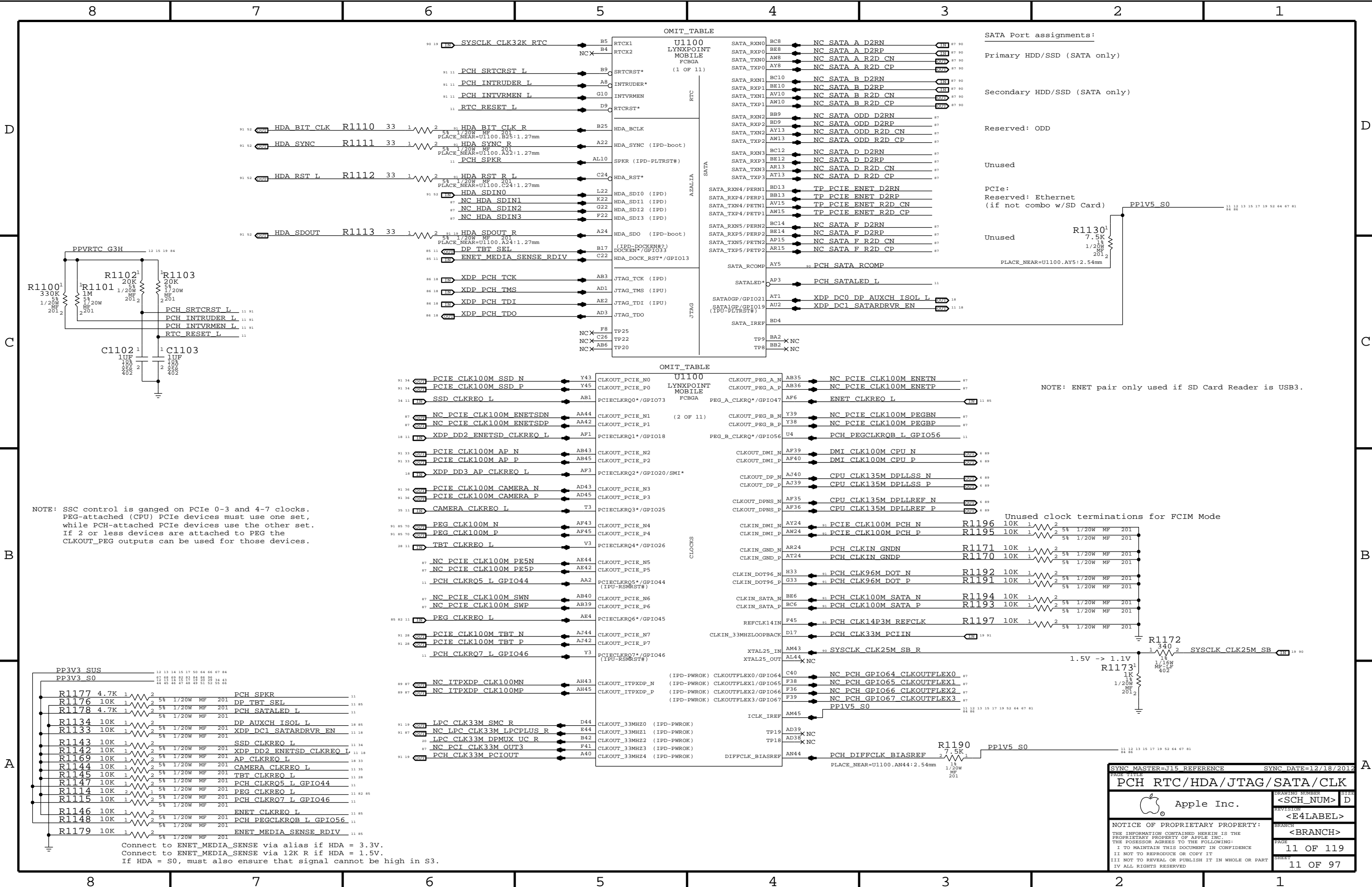








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NOTE: SSC control is ganged on PCIe 0-3 and 4-7 clocks. PEG-attached (CPU) PCIe devices must use one set, while PCH-attached PCIe devices use the other set. If 2 or less devices are attached to PEG the CLKOUT_PEG outputs can be used for those devices.

NOTE: ENET pair only used if SD Card Reader is USB3.

Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.

SYNC MASTER=J15 REFERENCE

SYNC DATE=12/18/2012

PCH RTC/HDA/JTAG/SATA/CLK

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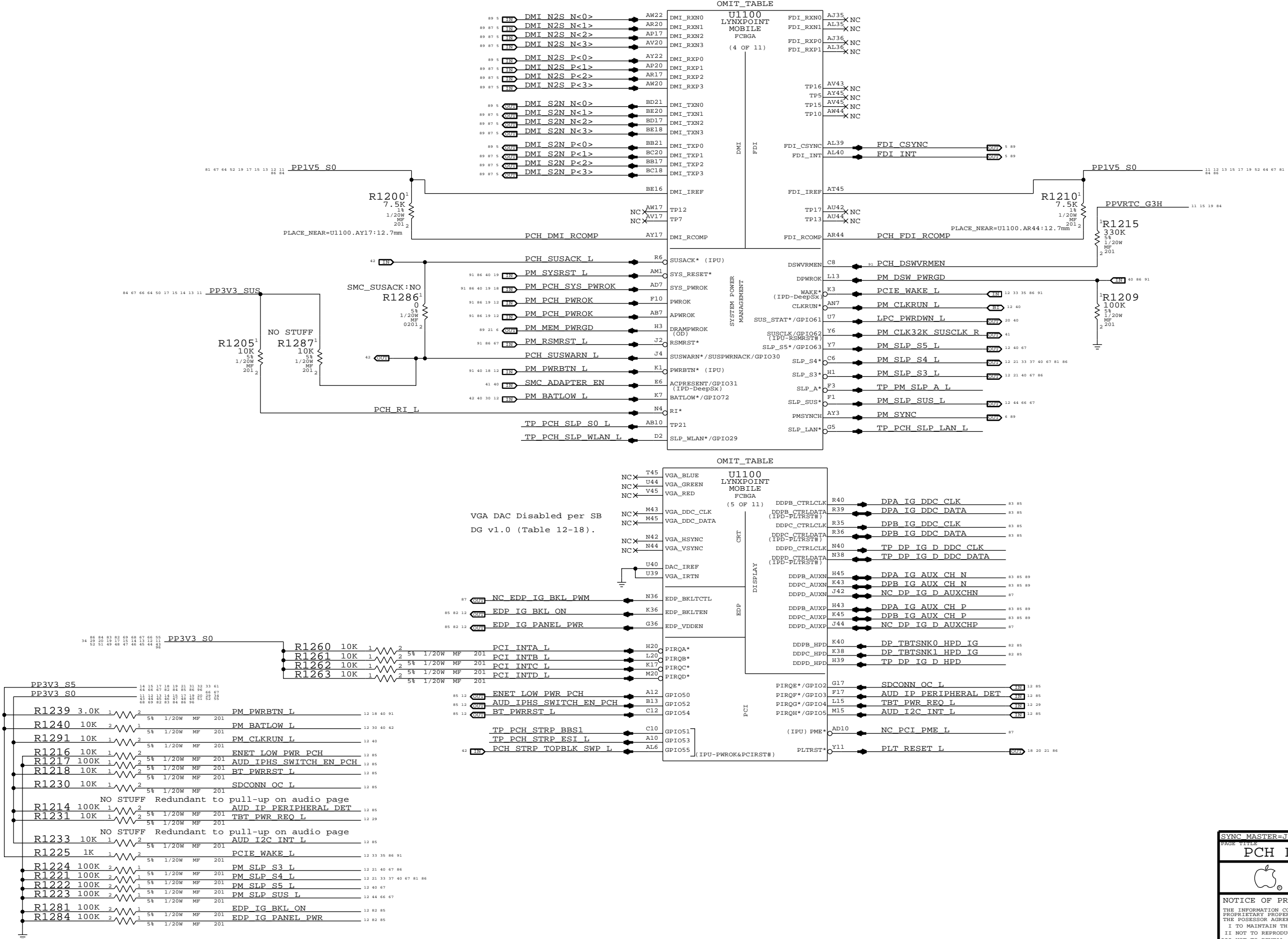
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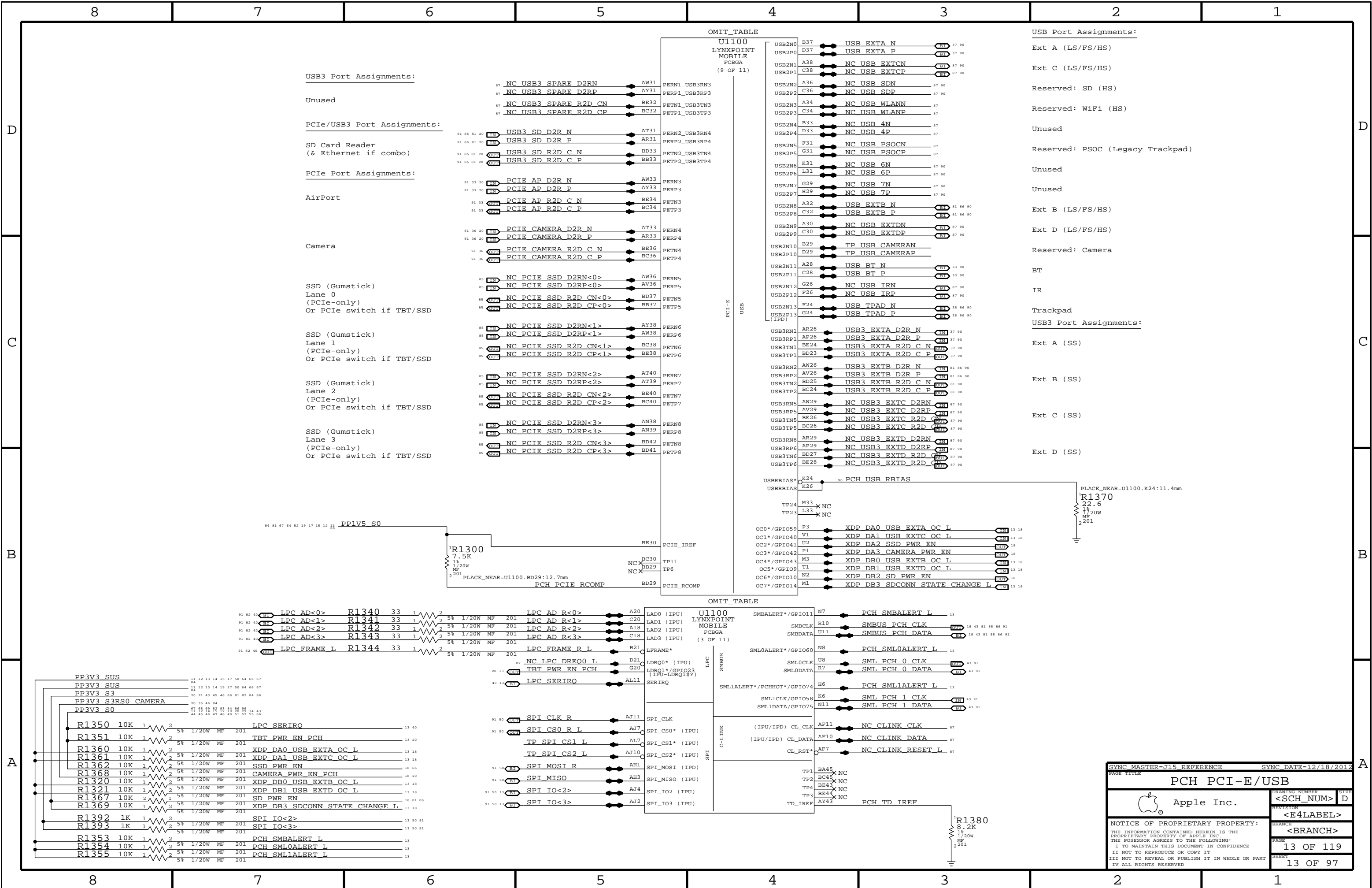
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Pull-up/down on chipset support page (depends on TBT controller)
Falcon Ridge: TBT_CIO_PLUG_EVENT_L, requires pull-up (S0), no isolation necessary.
Cactus Ridge: TBT_CIO_PLUG_EVENT, requires pull-down & isolation.

D

D

C

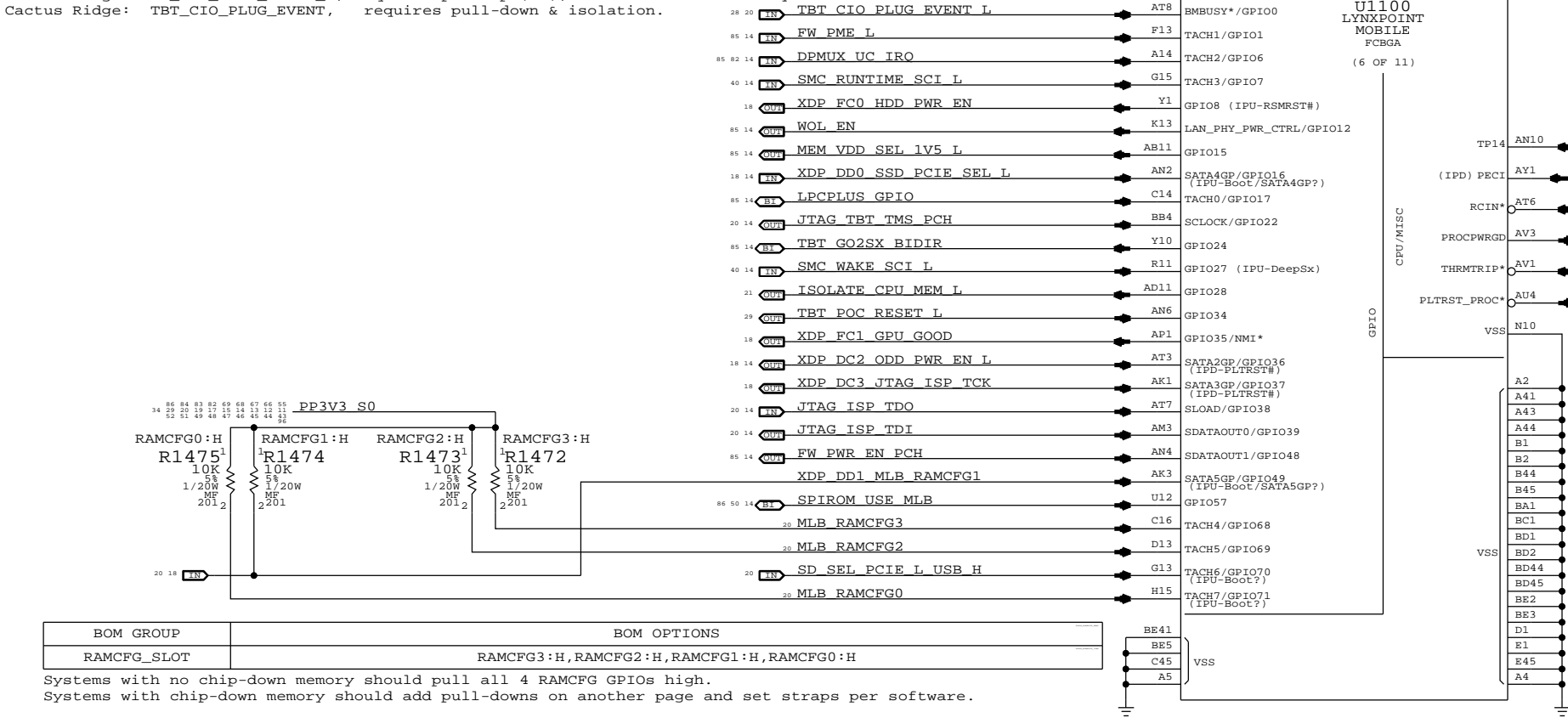
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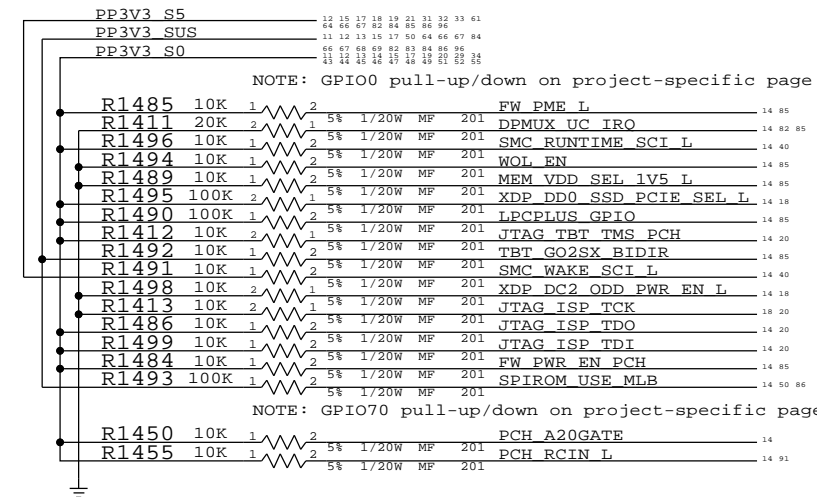
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A

A



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	1	RES,MF,1A MAX,0.0 OHM,5%,0201,BLACK	R1456		BDW_SPRT



SYNC MASTER=CLEAN X425

SYNC DATE=10/31/2014

PCH GPIO/MISC/NCTF

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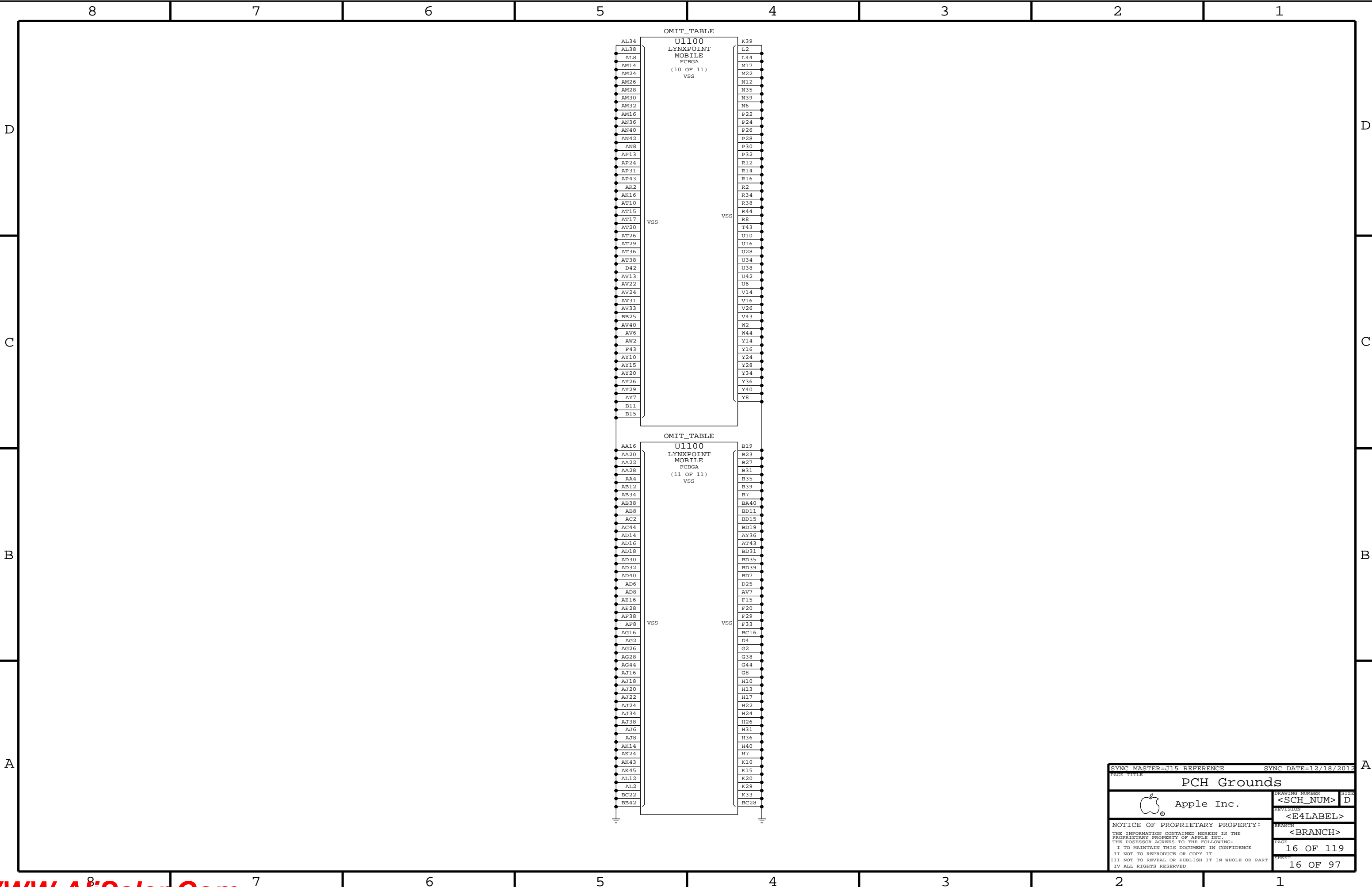
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SYNC MASTER=J15 REFERENCE

SYNC DATE=12/18/2012

PCH Grounds

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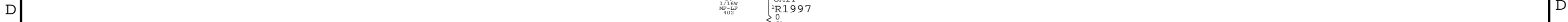
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DGII, DWPOK, Generation



NOTE: ALL_SYS_PWRGD must remain low until at least 5ms after all rails are valid.

```

06 03 82 69 58 07 66 55 52      DDMMYY SS
                                BYPASS=U1950::5MOM
                                C1 OF 0
                                PM DCH DWROK
                                VCCST (1.05V S0) PWBGD

```



FCM 55MHz CLOCKS



PCIE ME Disable Strap

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Camera power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

GreenClk 25MHz Power No bypass necessary

SB XTAL Power PP3V3 S5

Camera XTAL Power PP1V5 S0

TBT XTAL Power PP1V2 CAM XTALPCIEVDD

PP3V3 TBTLC

NC 2 VDD 5 HOT 13 VBAT and +V3.3A are

DMN5L06VK-7 SOT563 VER 5

PP1V5 S0

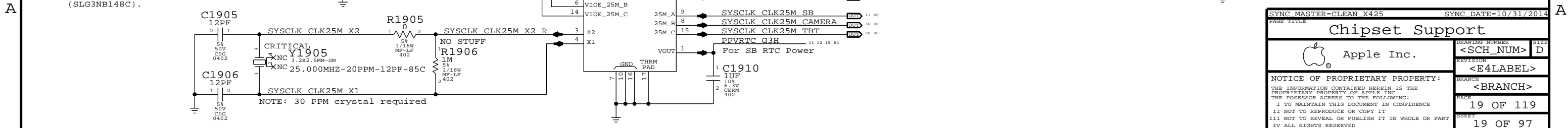
SPI_DESCRIPTOR_OVERRIDE LS5V

SPI_DESCRIPTOR_OVERRIDE

01820

DMN5L06VK-7

R1921

[illegible]

B	PCH ME Disable Strap	B
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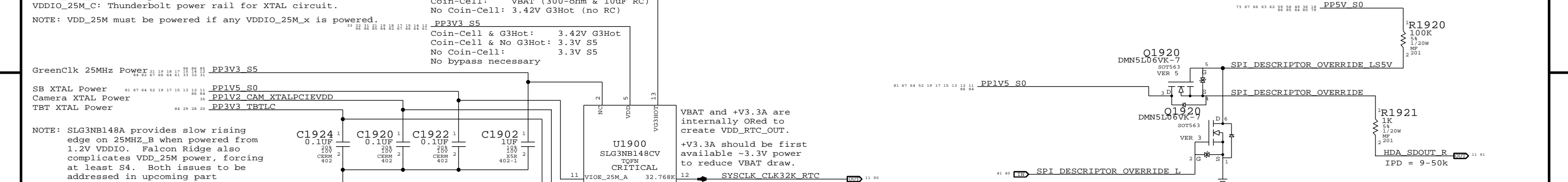
System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.

VDDIO_25M_B: Camera power rail for XTAL circuit.

PP3V42_G3H

Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.



SYNCH MASTER=CLEAN X425 SYNCH DATE=10/31/2014

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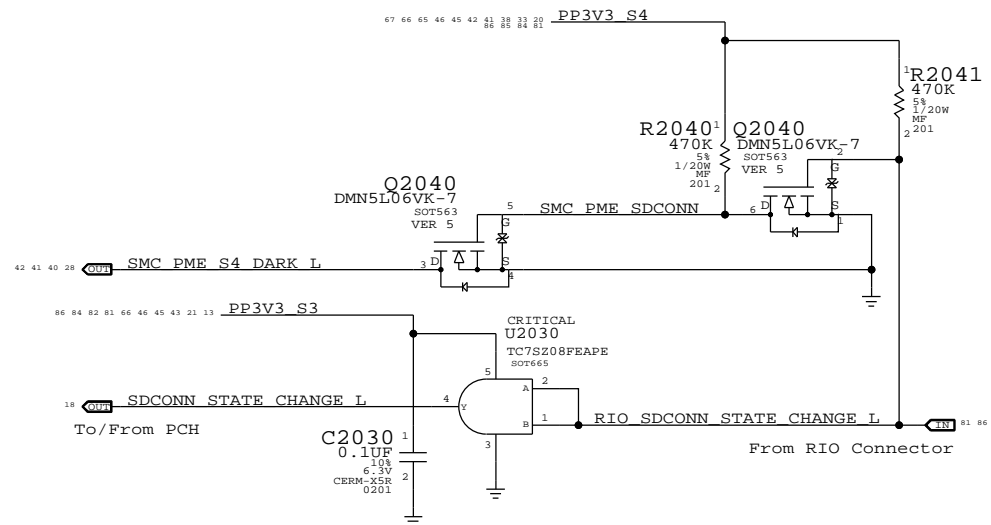
Chipset Support

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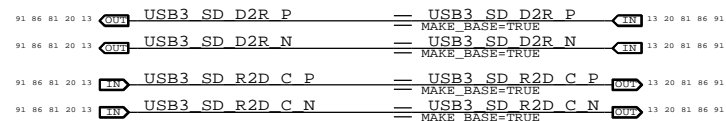
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RIO SD Card Reader Support



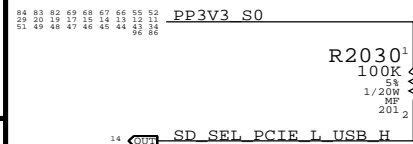
Flexible I/O Aliases

SD Card Reader is always USB3 in this implementaton.



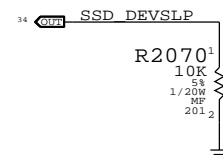
Flexible I/O Configuration Strap

Must pull signal correctly even if always USB or PCIe

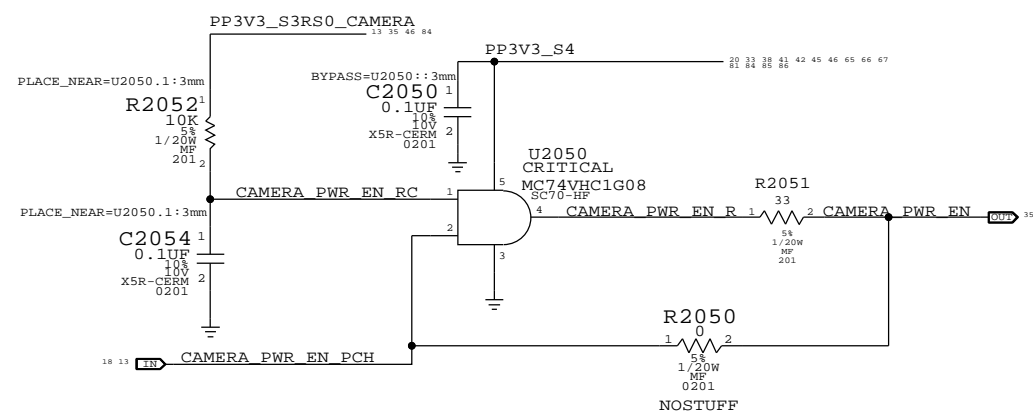


GS3 Connector Support

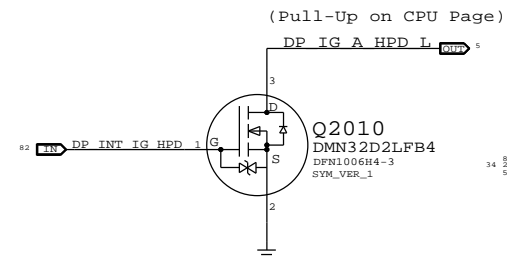
DEVSLP not supported on LPT-H



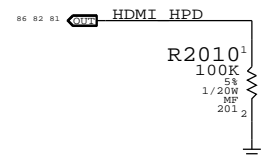
Camera power-up sequencing Support



LCD HPD Inverter

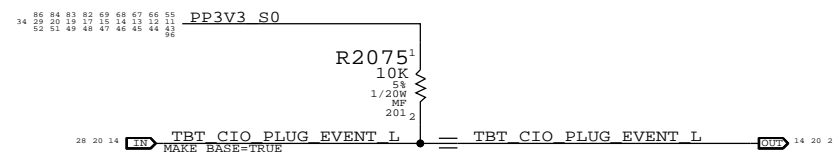


HDMI HPD pull-down



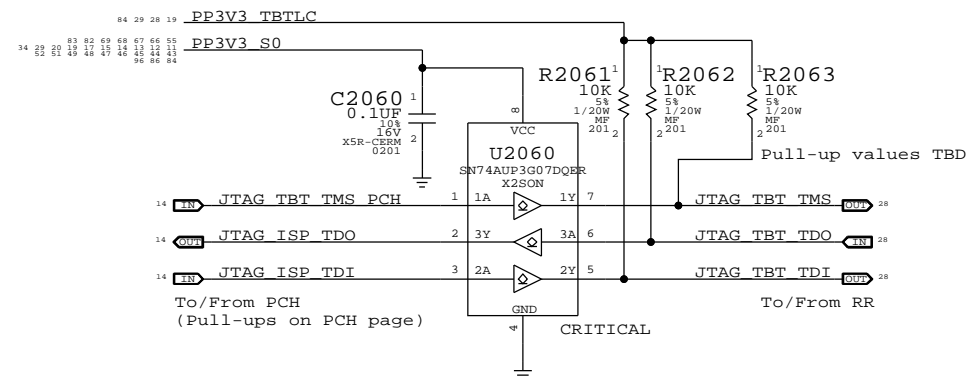
Falcon Ridge Support

RR output is open-drain, no isolation necessary

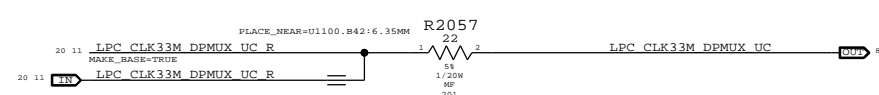


Falcon Ridge JTAG Isolation

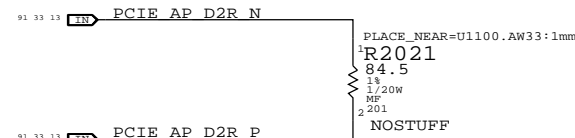
TBTLIC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH
U2060 supports I/O's powered when VCC=0V



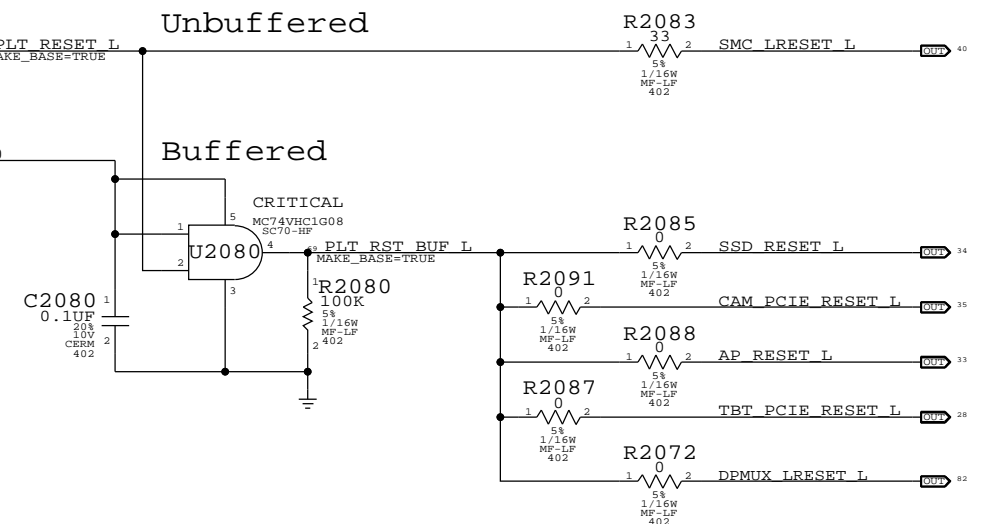
PCH 33MHz Clock for DPMUX



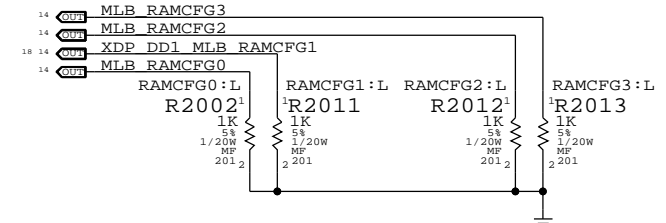
AP PCIE D2R test points



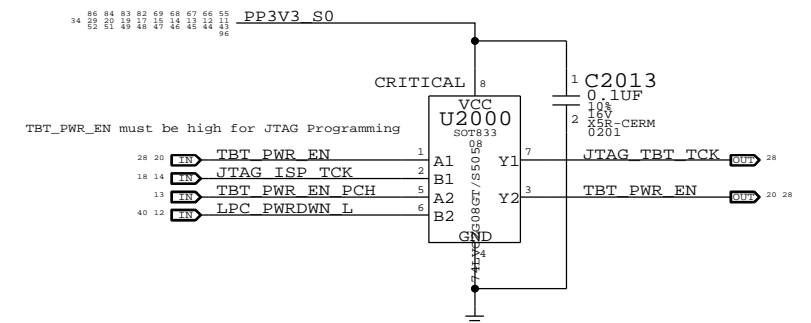
Platform Reset Connections



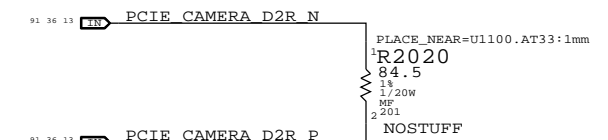
RAM Configuration Straps




GPIO Glitch Prevention



Camera PCIe D2R test points

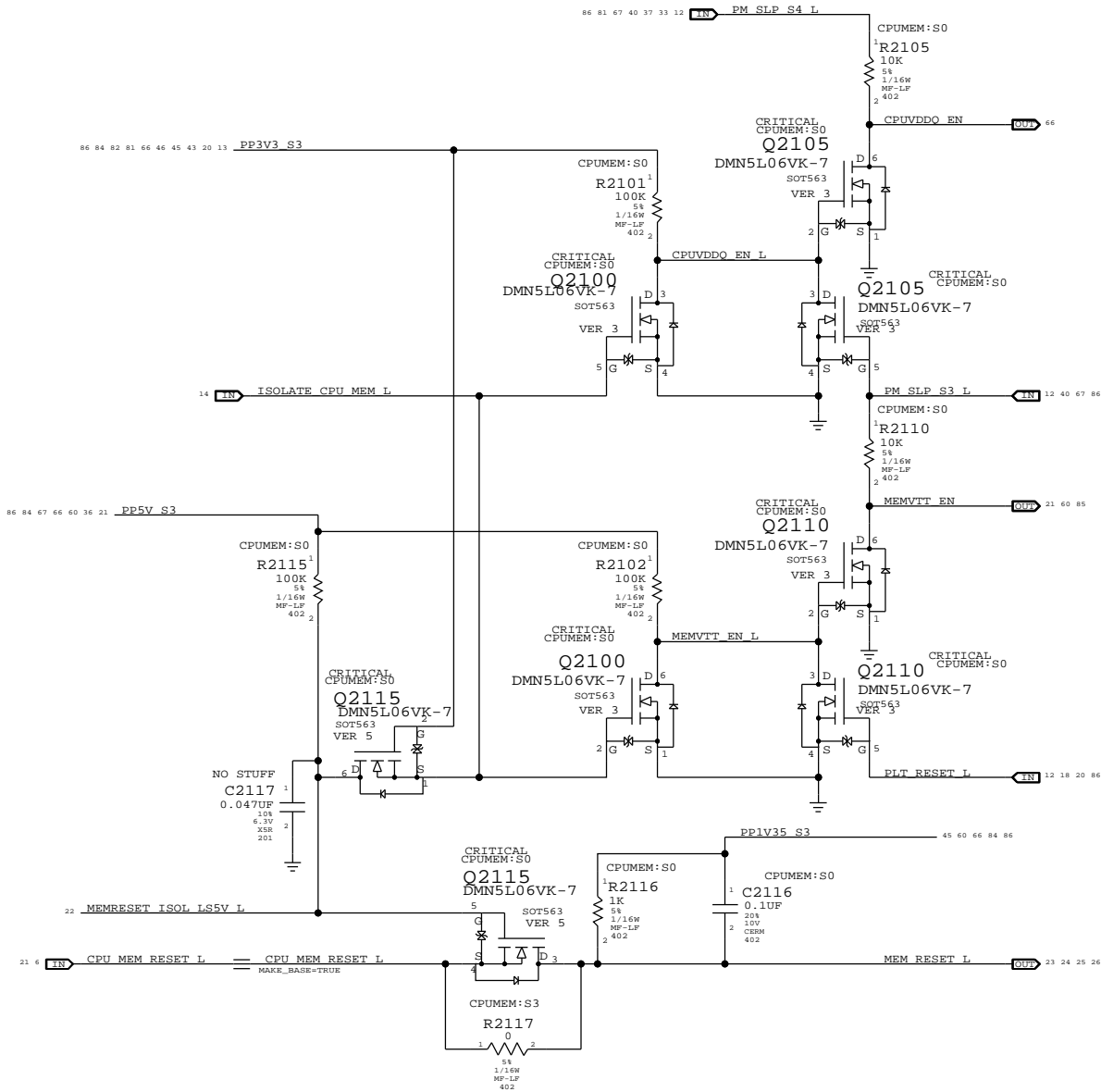


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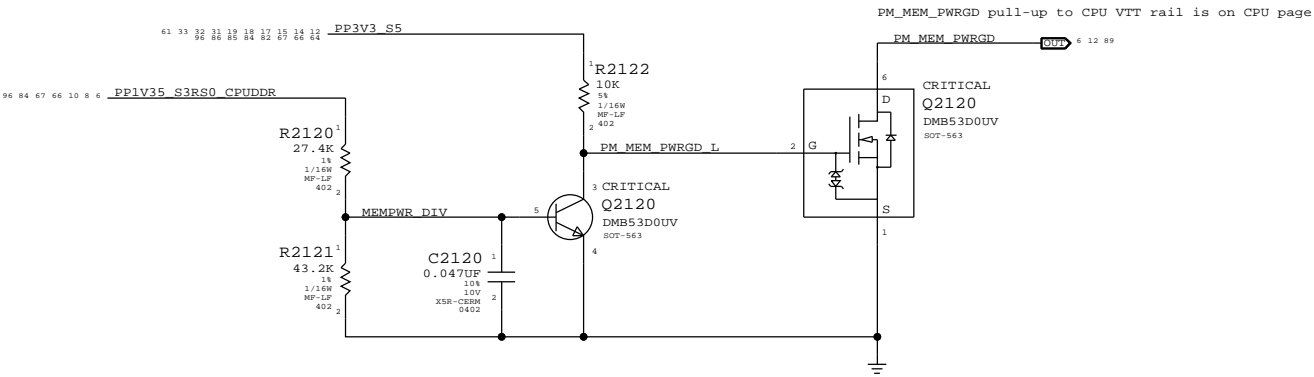
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

CPUVDDQ_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

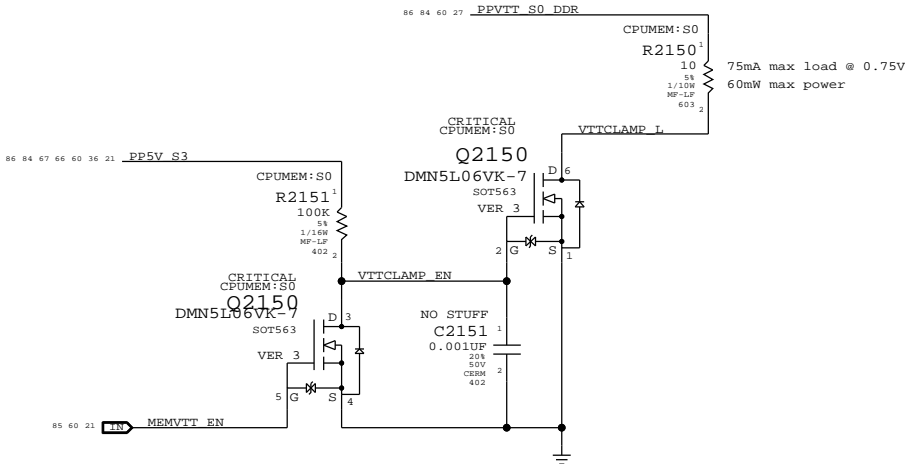


MEM S0 "PGOOD" for CPU



MEMVTT Clamp


Ensures CKE signals are held low in S3



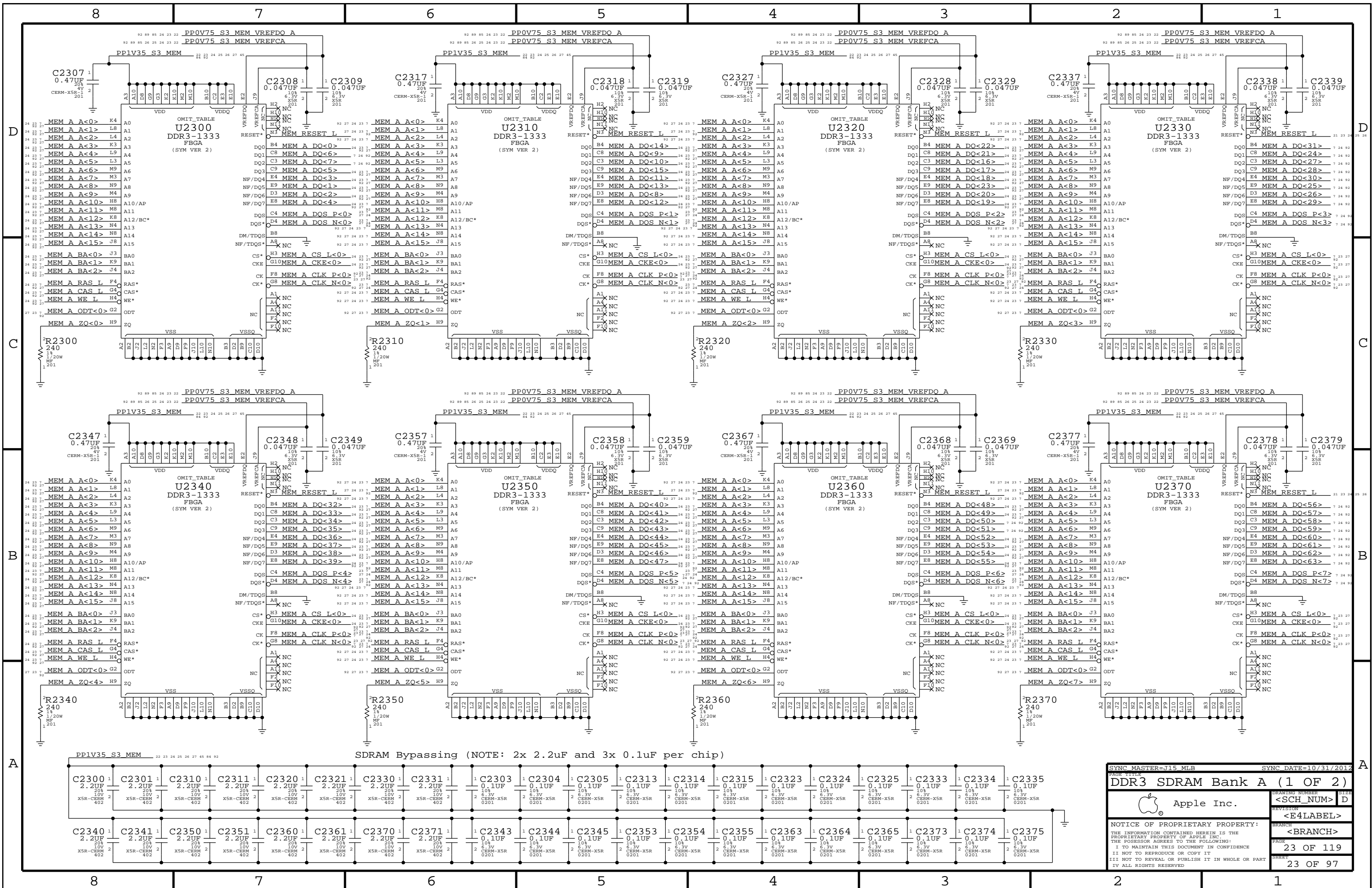
Step	SOLATE_CPU_MEM_L	PLT_RST_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	CPUVDDQ_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
1	1	0	1	1	1	1	1	1
to	2	0	0	1	1	1	0	1
3	0	0	0	1	X	1	0	0
S3	4	0	0	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
to	6	0	1	1	1	1	1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1


(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

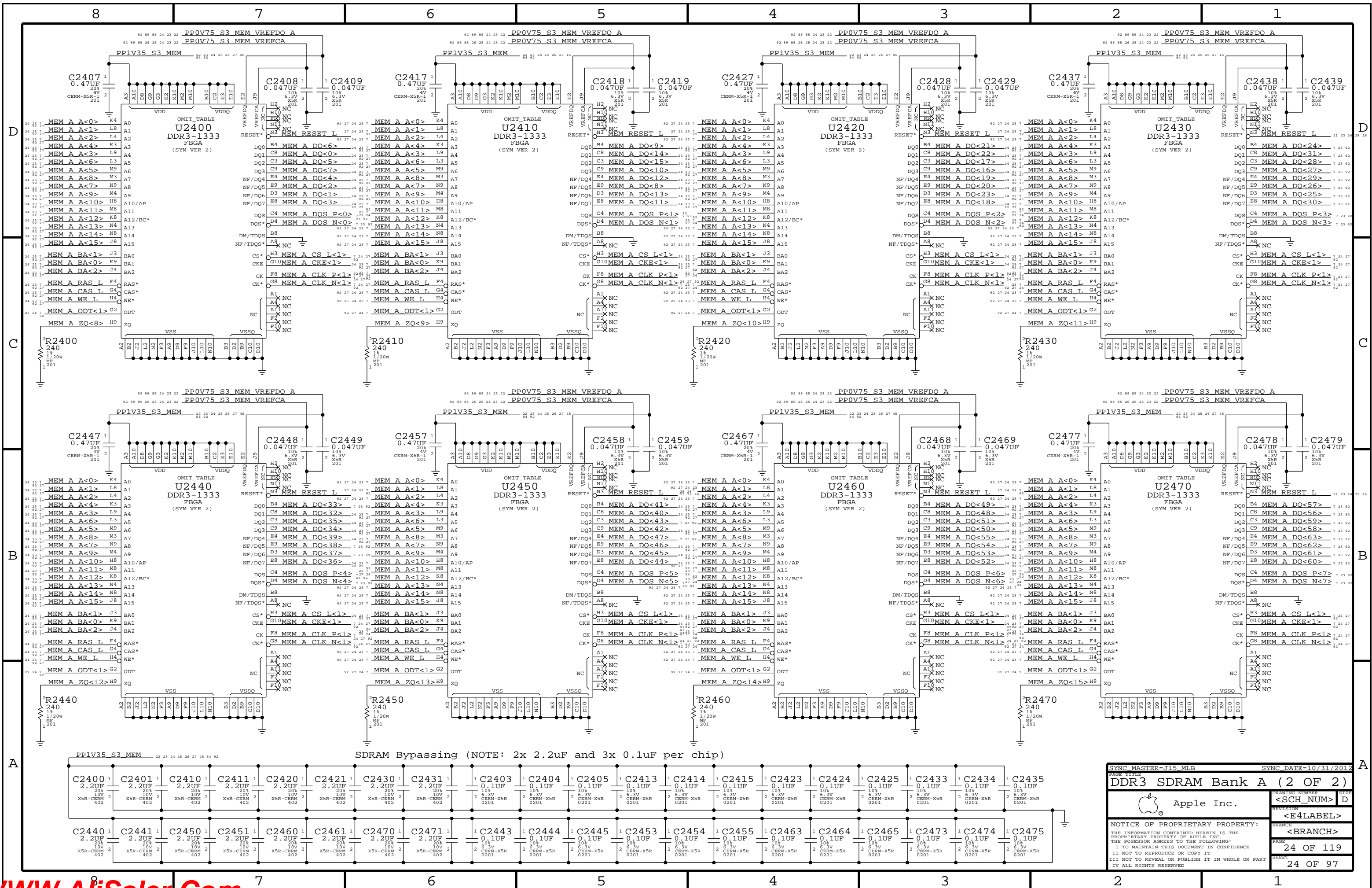
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.


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CPU Memory S3 Support			
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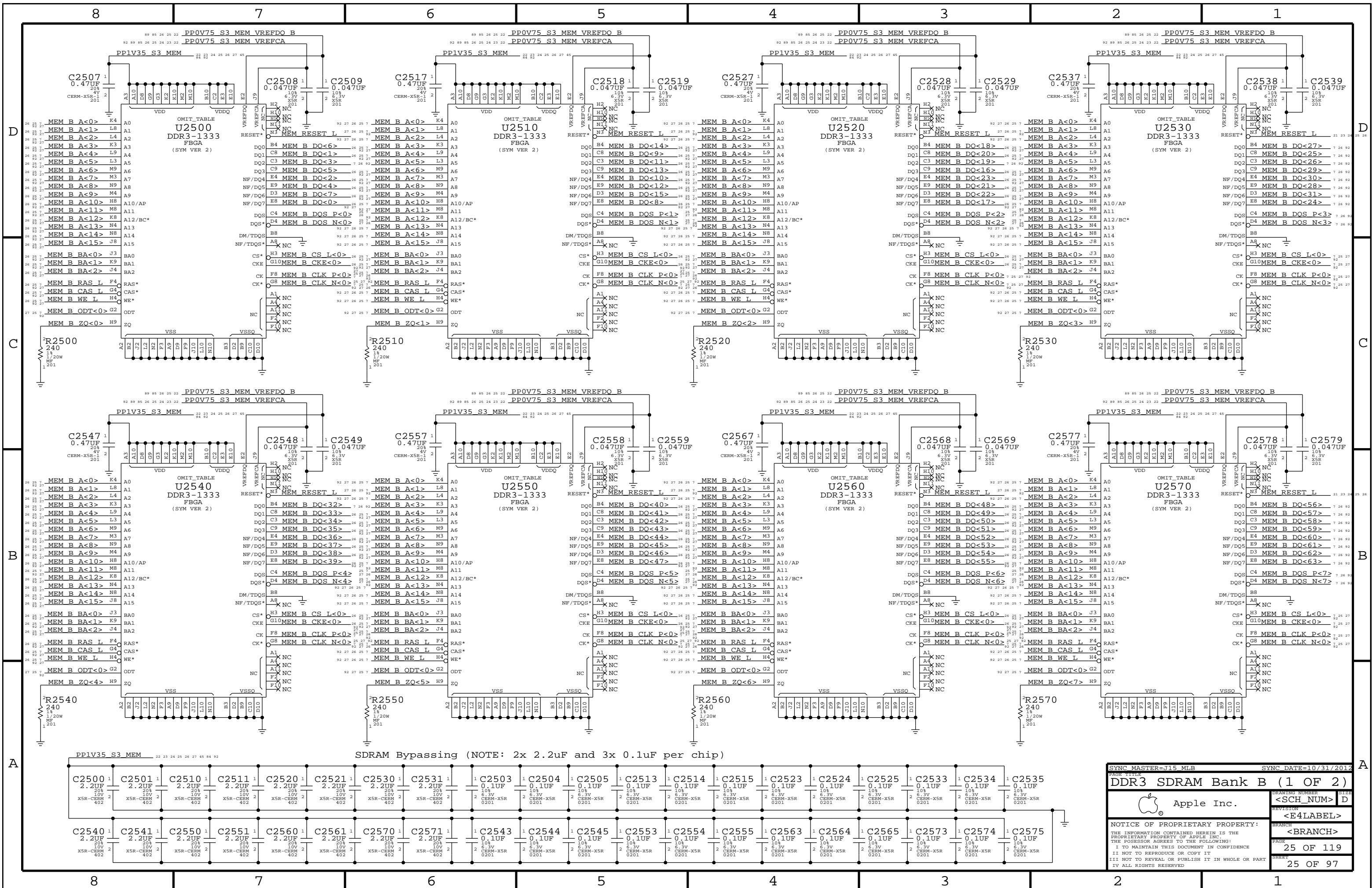
NOTE: CPU has single output for VREFCA.
Connected to 4 DRAMs.



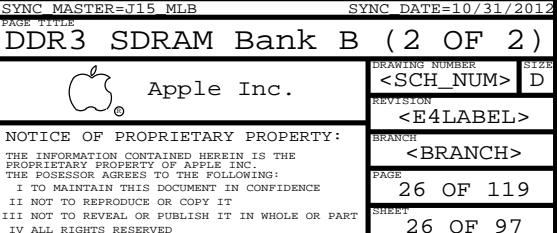
SYNC MASTER=J15 MLB		SYNC DATE=10/31/2012	
PAGE TITLE			
DDR3 SDRAM Bank A (1 OF 2)			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
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		PAGE	23 OF 119
		SHEET	23 OF 97

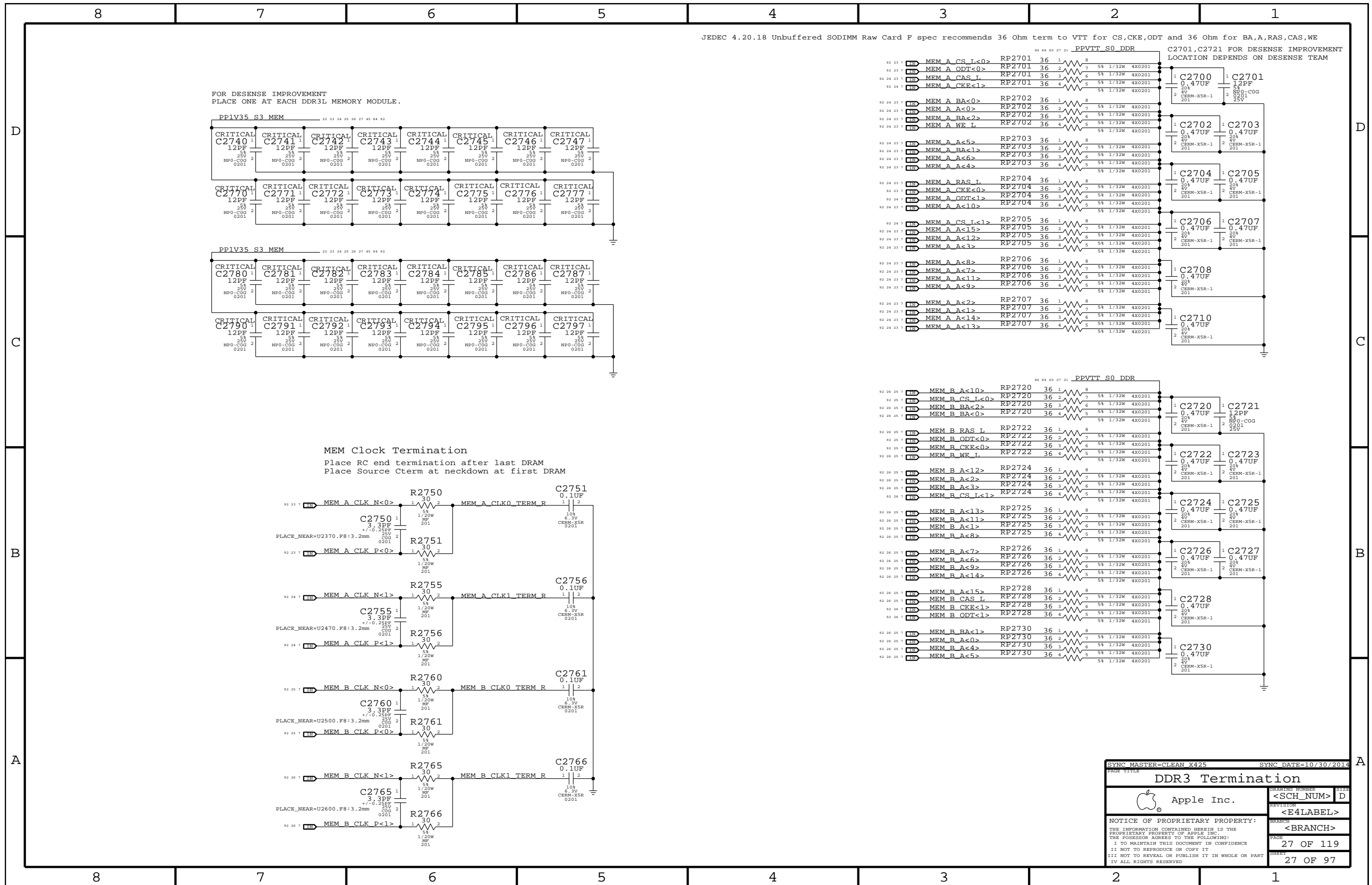


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DDR3 SDRAM Bank A (2 OF 2)			
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		PAGE 24 OF 119	
		SHEET 24 OF 97	

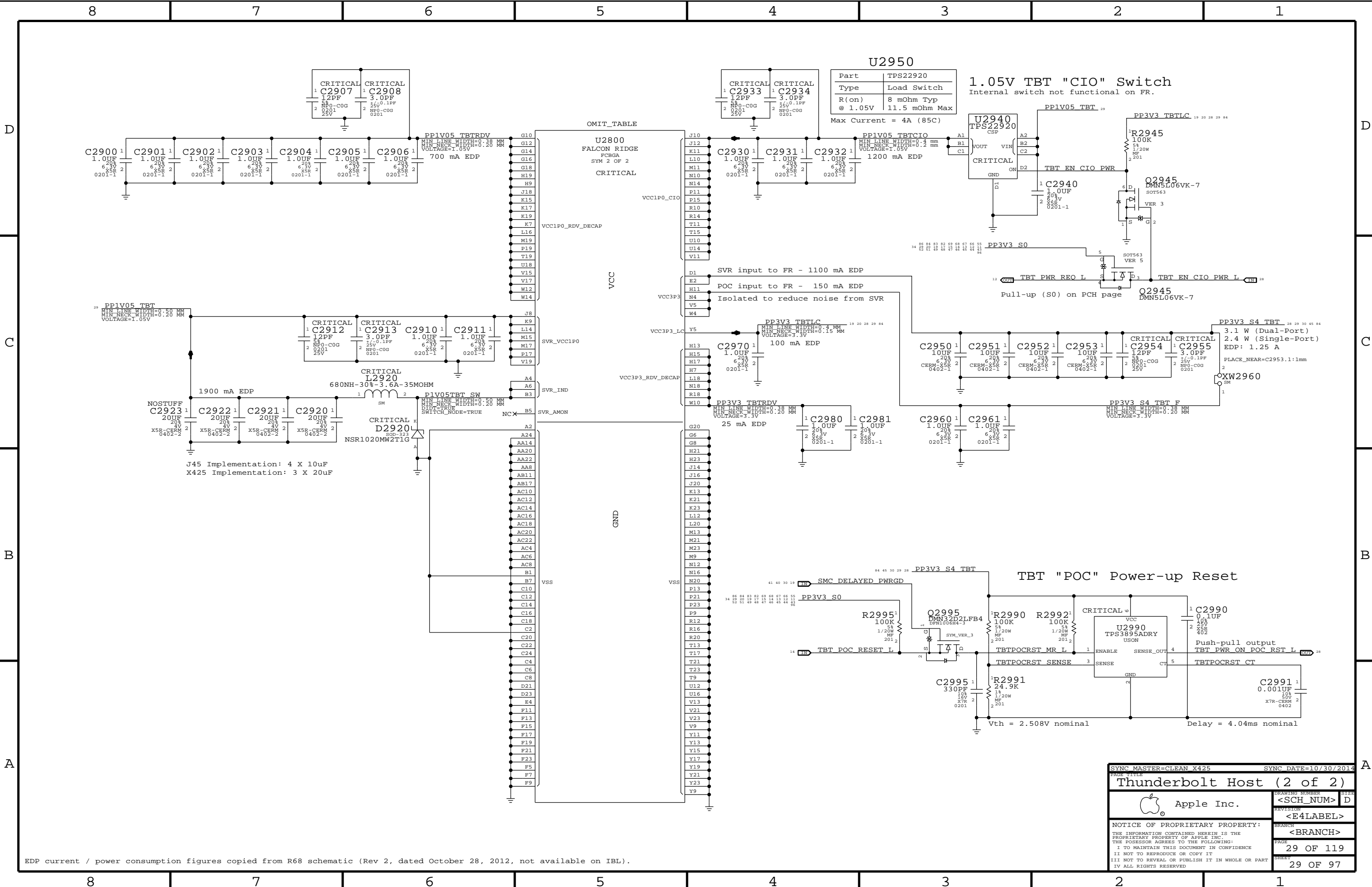


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Apple Inc.
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25 OF 119
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25 OF 97
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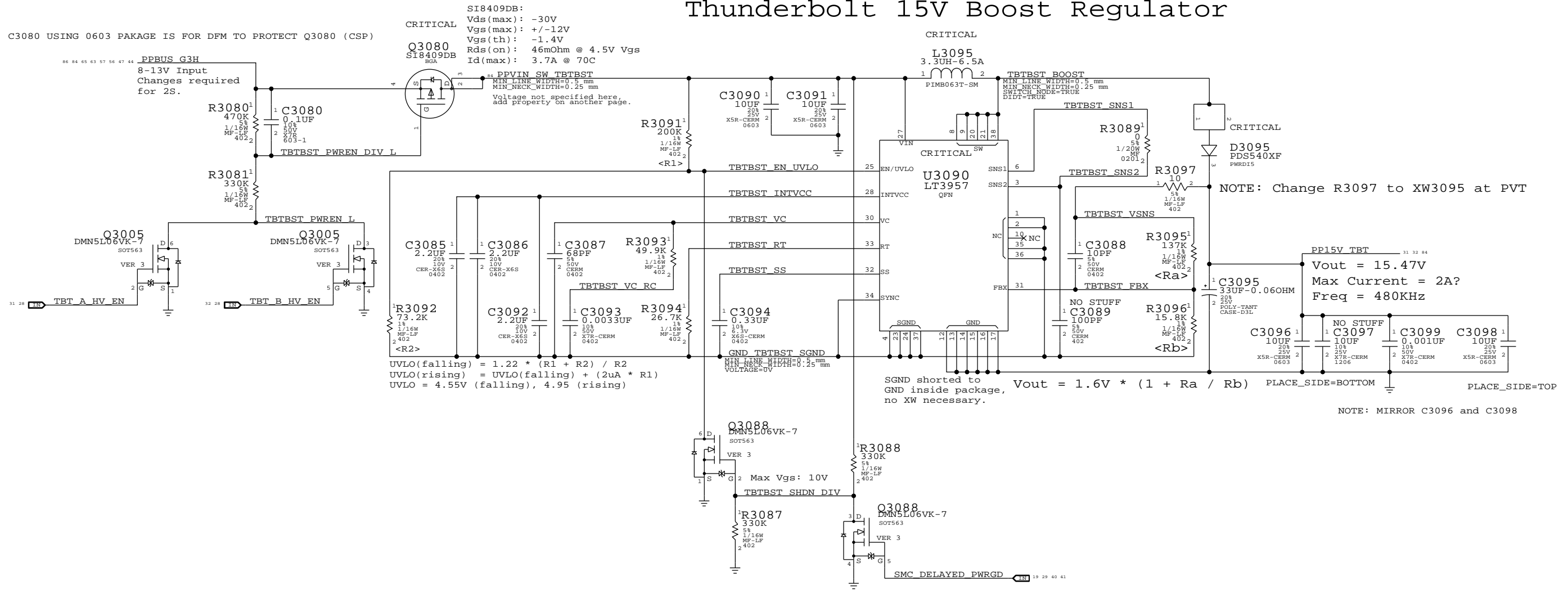
EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

SYNC MASTER=CLEAN X425		SYNC DATE=10/30/2014	
PAGE TITLE		Thunderbolt Host (2 of 2)	
 Apple Inc.		DRAWING NUMBER	SIZE
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		PAGE	29 OF 119
		SHEET	29 OF 97

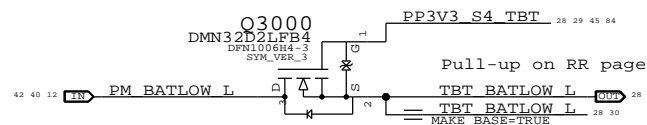
Page Notes


Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)

Thunderbolt 15V Boost Regulator



BATLOW# Isolation



SYNC MASTER=CLEAN X305		SYNC DATE=06/24/2014	
PAGE TITLE			
Thunderbolt Mobile Support			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
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8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

D



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

B



D



A

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

D



C

B

A



4



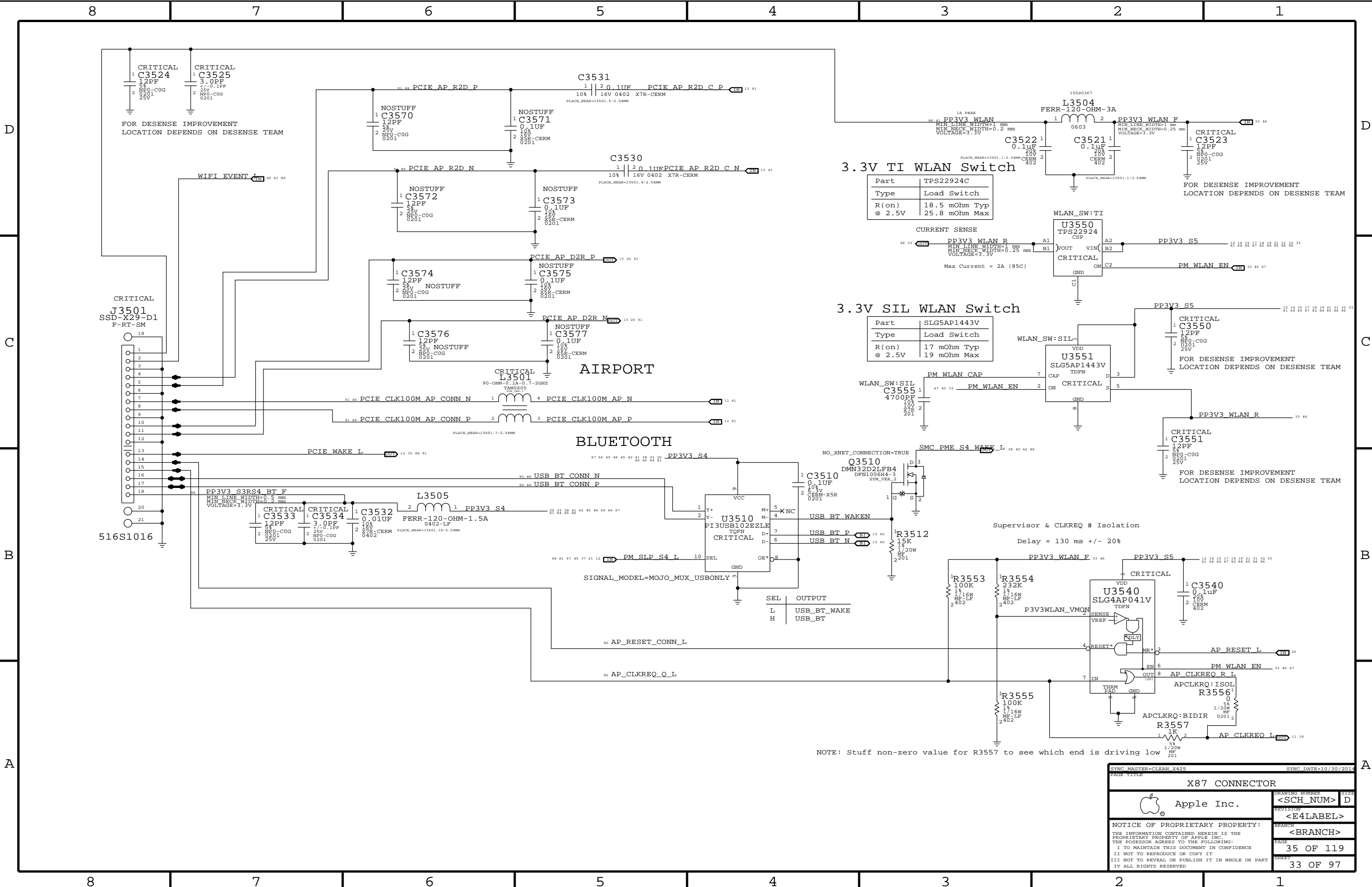
D



B

A

1



D

C

B

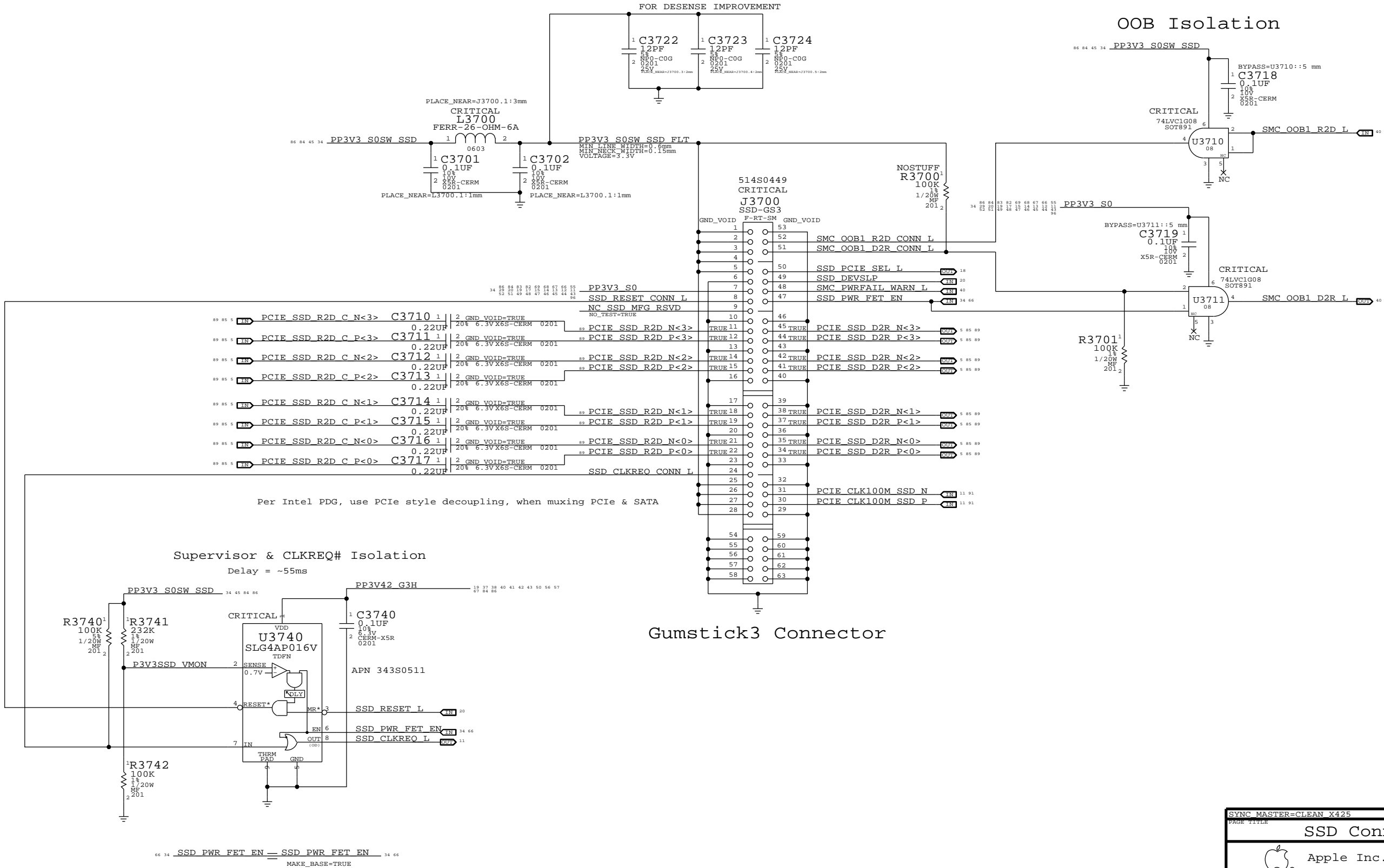
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D

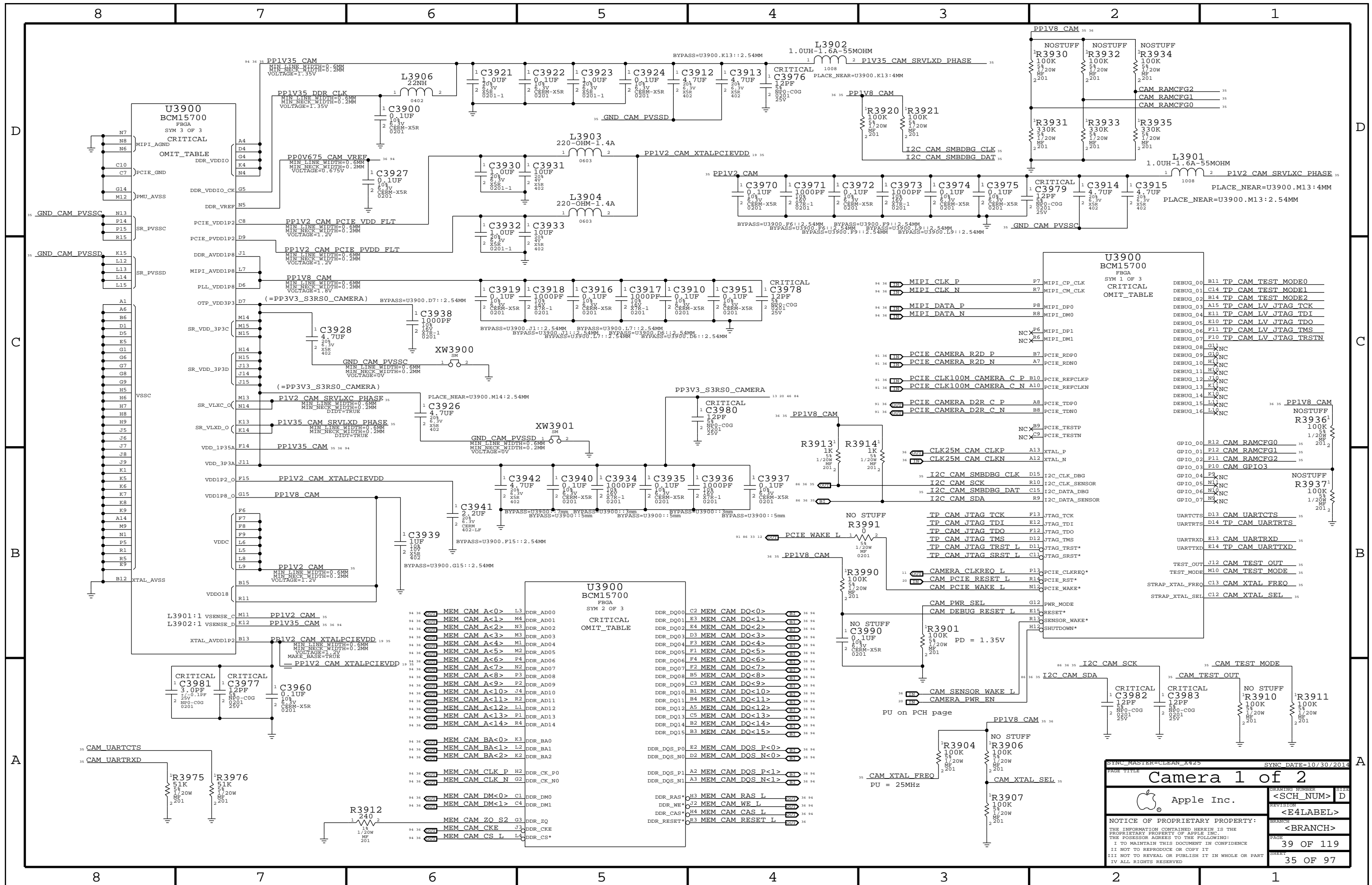
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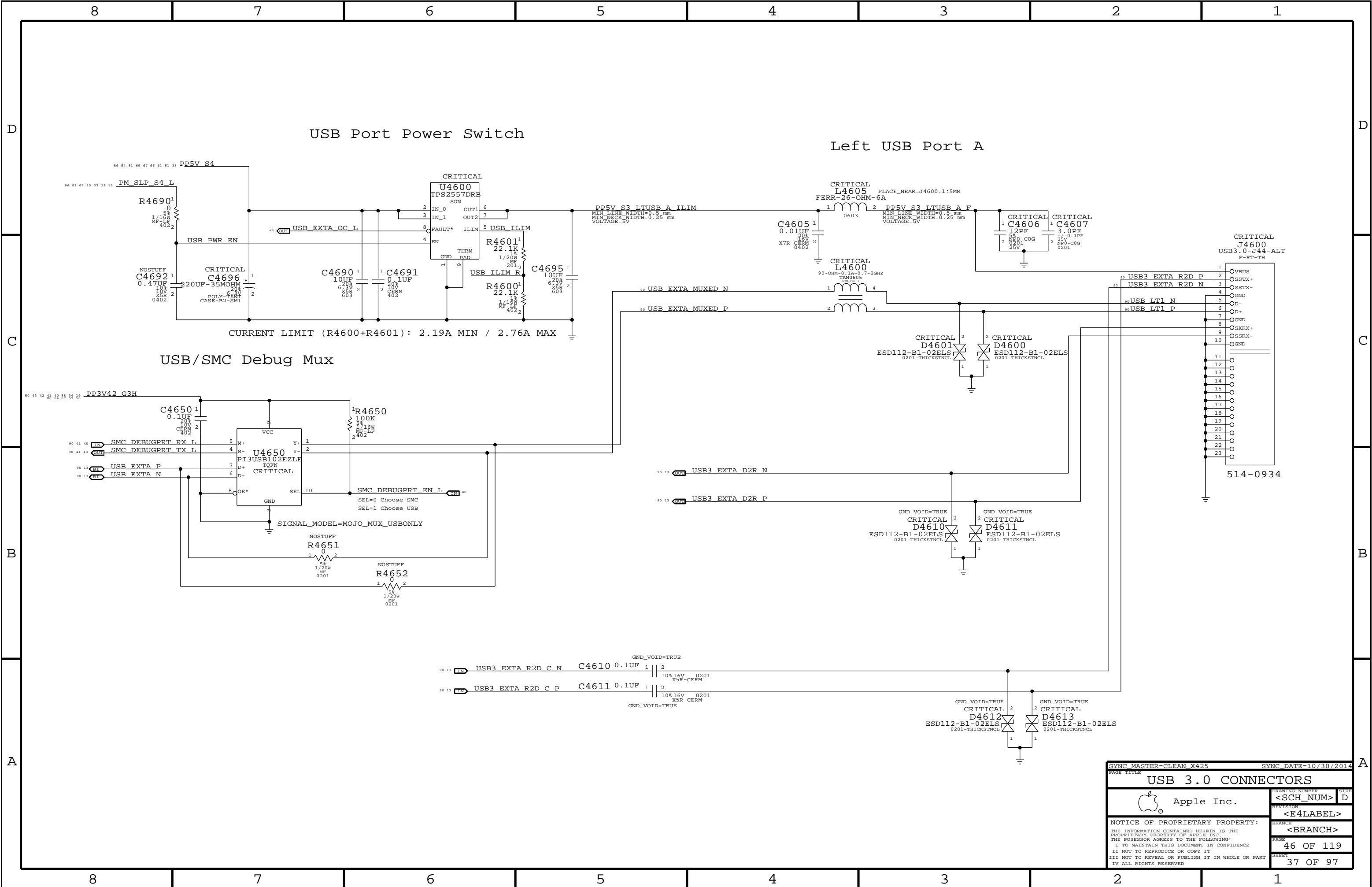
B

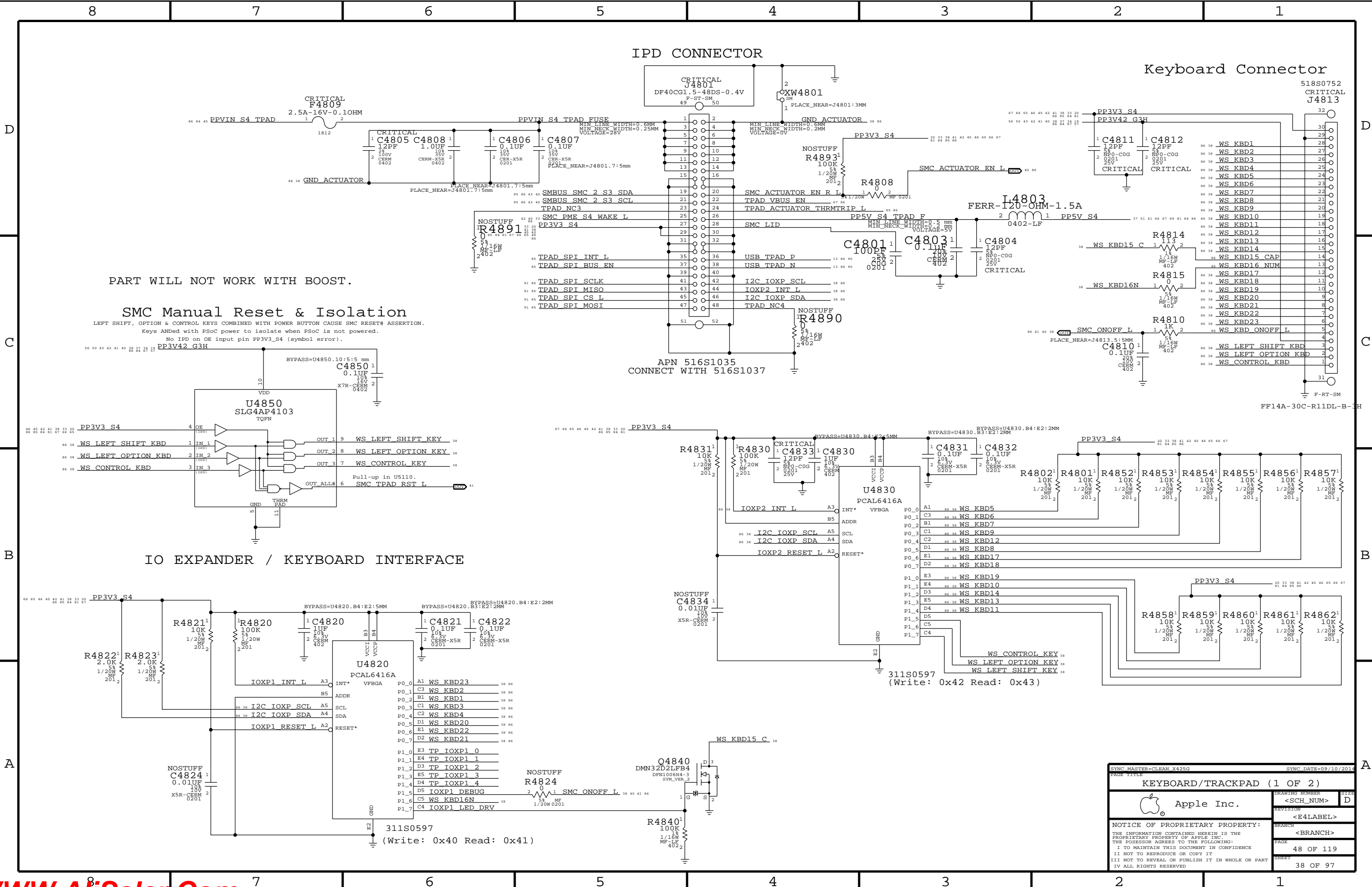
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SYNC MASTER=CLEAN X425		SYNC DATE=08/15/2014	
PAGE TITLE			
SSD Connector			
 Apple Inc.		DRAWING NUMBER	SIZE
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		<BRANCH>	
		PAGE	37 OF 119
		SHEET	34 OF 97








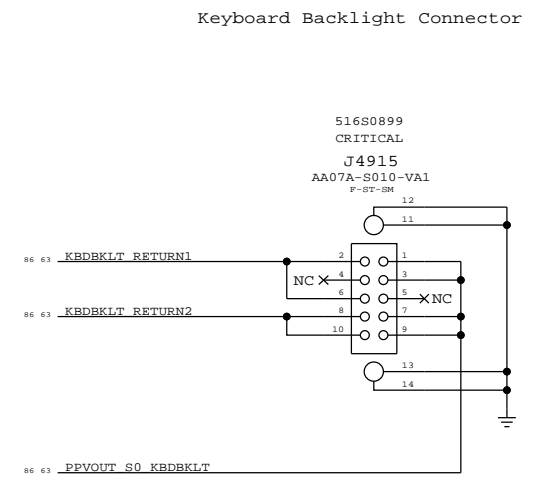
PART WILL NOT WORK WITH BOOST.


SMC Manual Reset & Isolation

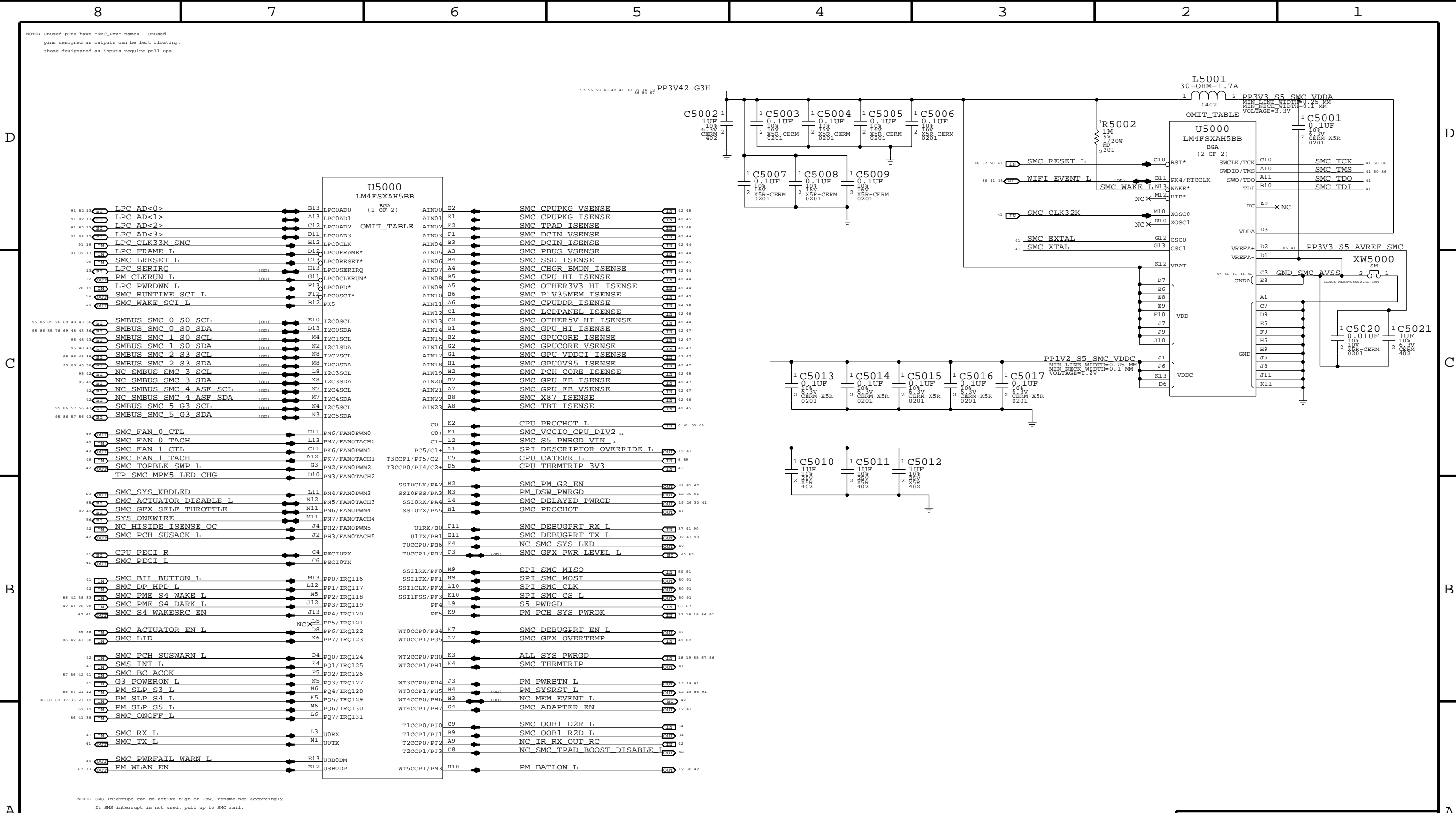
LEFT SHIFT, OPTION & CONTROL KEYS COMBINED WITH POWER BUTTON CAUSE SMC RESET# ASSERTION.
Keys ANDed with PSoC power to isolate when PSoC is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).

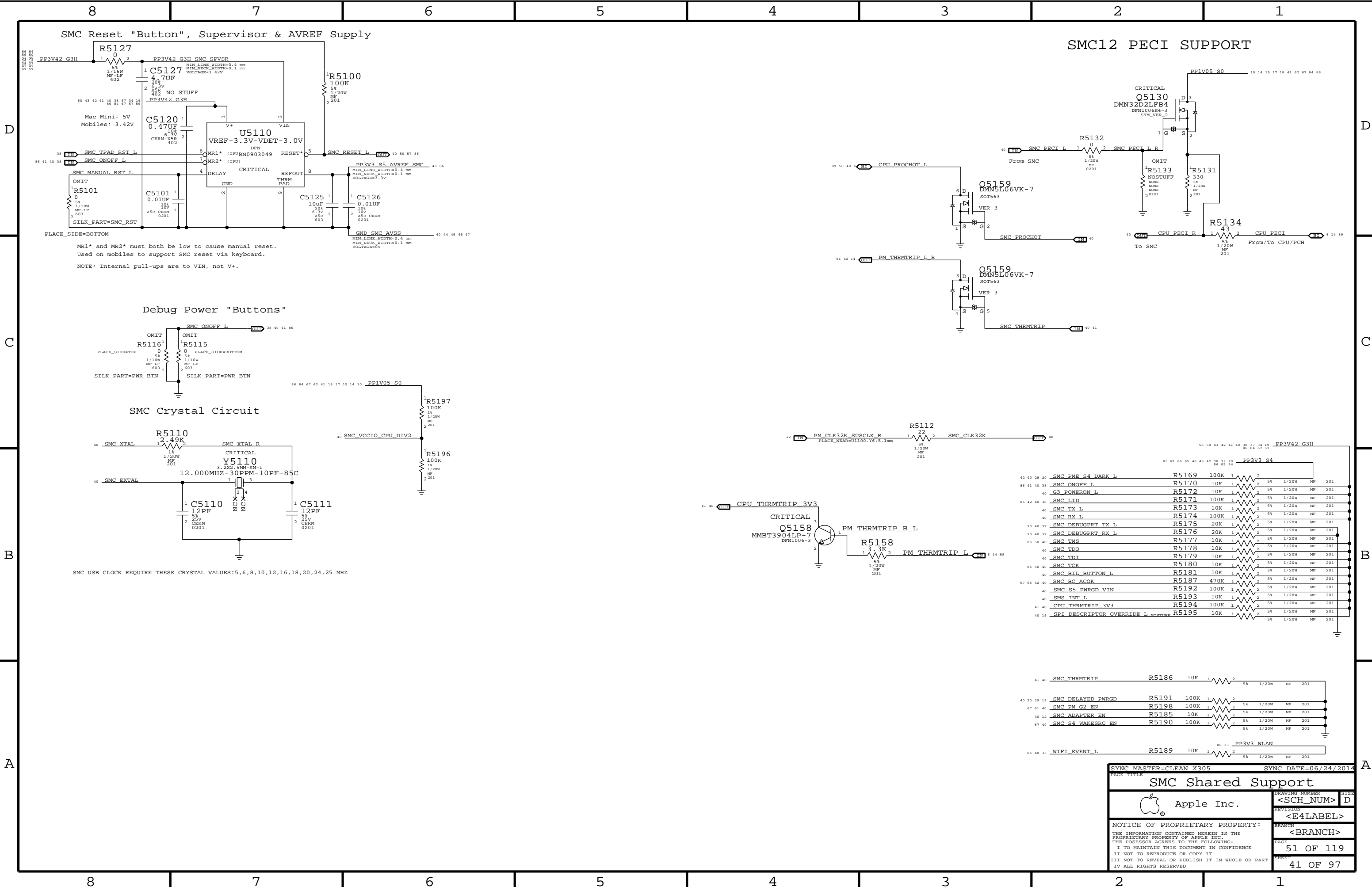
IO EXPANDER / KEYBOARD INTERFACE

SYNC MASTER=CLEAN X42SG		SYNC DATE=09/10/2014	
PAGE TITLE			
KEYBOARD/TRACKPAD		(1 OF 2)	
 Apple Inc.	DRAWING NUMBER		SIZE
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SYNC MASTER=CLEAN MAXWELL PAGE TITLE		SYNC DATE=07/02/2014		A
KEYBOARD/TRACKPAD (2 OF 2)				
 Apple Inc.		DRAWING NUMBER <SCH_NUM>		
		SIZE D		
		REVISION <E4LABEL>		
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D

C

B

A

D

C

B

A

57 56 42 41 40

SMC BC ACOK

=

SMC BC ACOK

MAKE_BASE=TRUE

40 41 42 56 57

42 40

NC HISIDE ISENSE OC

=

NC HISIDE ISENSE OC

MAKE_BASE=TRUE NO_TEST=TRUE

40 42

45 42 40

SMC CPUPKG VSENSE

=

SMC CPUPKG VSENSE

MAKE_BASE=TRUE

40 42 45

45 42 40

SMC CPUPKG ISENSE

=

SMC CPUPKG ISENSE

MAKE_BASE=TRUE

40 42 45

45 42 40

SMC TPAD ISENSE

=

SMC TPAD ISENSE

MAKE_BASE=TRUE

40 42 45

44 42 40

SMC DCIN VSENSE

=

SMC DCIN VSENSE

MAKE_BASE=TRUE

40 42 44

44 42 40

SMC DCIN ISENSE

=

SMC DCIN ISENSE

MAKE_BASE=TRUE

40 42 44

44 42 40

SMC PBUS VSENSE

=

SMC PBUS VSENSE

MAKE_BASE=TRUE

40 42 44

45 42 40

SMC SSD ISENSE

=

SMC SSD ISENSE

MAKE_BASE=TRUE

40 42 45

44 42 40

SMC CHGR BMON ISENSE

=

SMC CHGR BMON ISENSE

MAKE_BASE=TRUE

40 42 44

44 42 40

SMC CPU HI ISENSE

=

SMC CPU HI ISENSE

MAKE_BASE=TRUE

40 42 44

44 42 40

SMC OTHER3V3 HI ISENSE

=

SMC OTHER3V3 HI ISENSE

MAKE_BASE=TRUE

40 42 44

45 42 40

SMC P1V35MEM ISENSE

=

SMC P1V35MEM ISENSE

MAKE_BASE=TRUE

40 42 45

46 42 40

SMC CPUDDR ISENSE

=

SMC CPUDDR ISENSE

MAKE_BASE=TRUE

40 42 46

46 42 40

SMC LCDPANEL ISENSE

=

SMC LCDPANEL ISENSE

MAKE_BASE=TRUE

40 42 46

44 42 40

SMC OTHER5V HI ISENSE

=

SMC OTHER5V HI ISENSE

MAKE_BASE=TRUE

40 42 44

47 42 40

SMC GPU HI ISENSE

=

SMC GPU HI ISENSE

MAKE_BASE=TRUE

40 42 47

47 42 40

SMC GPUCORE ISENSE

=

SMC GPUCORE ISENSE

MAKE_BASE=TRUE

40 42 47

47 42 40

SMC GPUCORE VSENSE

=

SMC GPUCORE VSENSE

MAKE_BASE=TRUE

40 42 47

47 42 40

SMC GPU VDDCI ISENSE

=

SMC GPU VDDCI ISENSE

MAKE_BASE=TRUE

40 42 47

47 42 40

SMC GPU0V95 ISENSE

=

SMC GPU0V95 ISENSE

MAKE_BASE=TRUE

40 42 47

45 42 40

SMC PCH CORE ISENSE

=

SMC PCH CORE ISENSE

MAKE_BASE=TRUE

40 42 45

47 42 40

SMC GPU FB ISENSE

=

SMC GPU FB ISENSE

MAKE_BASE=TRUE

40 42 47

47 42 40

SMC GPU FB VSENSE

=

SMC GPU FB VSENSE

MAKE_BASE=TRUE

40 42 47

46 42 40

SMC X87 ISENSE

=

SMC X87 ISENSE

MAKE_BASE=TRUE

40 42 46

45 42 40

SMC TBT ISENSE

=

SMC TBT ISENSE

MAKE_BASE=TRUE

40 42 45

42 40

NC SMBUS SMC 4 ASF SCL

=

NC SMBUS SMC 4 ASF SCL

MAKE_BASE=TRUE NO_TEST=TRUE

40 42

42 40

NC SMBUS SMC 4 ASF SDA

=

NC SMBUS SMC 4 ASF SDA

MAKE_BASE=TRUE NO_TEST=TRUE

40 42

95 42 40

NC SMBUS SMC 3 SCL

=

NC SMBUS SMC 3 SCL

MAKE_BASE=TRUE NO_TEST=TRUE

40 42 95

95 42 40

NC SMBUS SMC 3 SDA

=

NC SMBUS SMC 3 SDA

MAKE_BASE=TRUE NO_TEST=TRUE

40 42 95

42 40

NC SMC TPAD BOOST DISABLE

=

NC SMC TPAD BOOST DISABLE

MAKE_BASE=TRUE NO_TEST=TRUE

40 42

42 41 40 28 20

SMC PME S4 DARK L

=

SMC PME S4 DARK L

MAKE_BASE=TRUE

20 28 40 41 42

42 41 40 28 20

SMC PME S4 DARK L

=

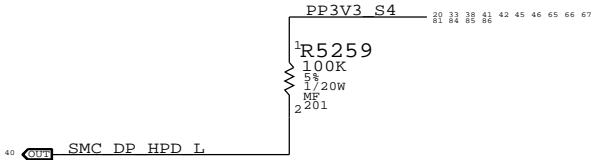
SMC PME S4 DARK L

MAKE_BASE=TRUE

20 28 40 41 42

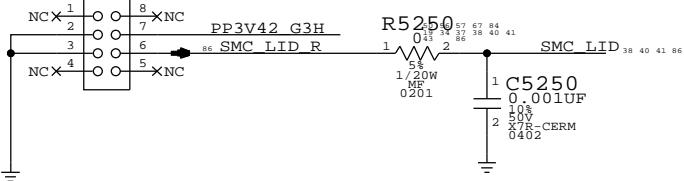
GPU HI ISENSE

Spare S4 IRQ

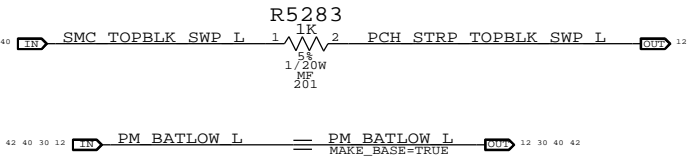
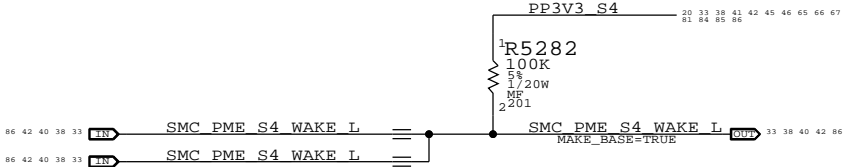
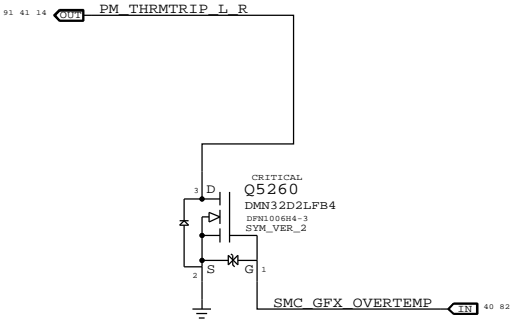
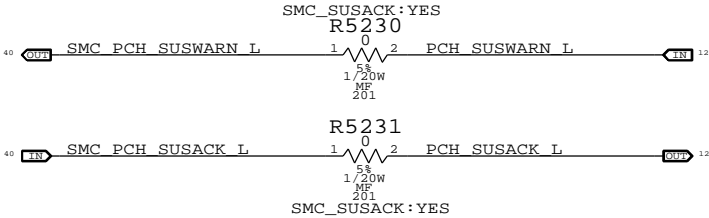


Hall Effect pads

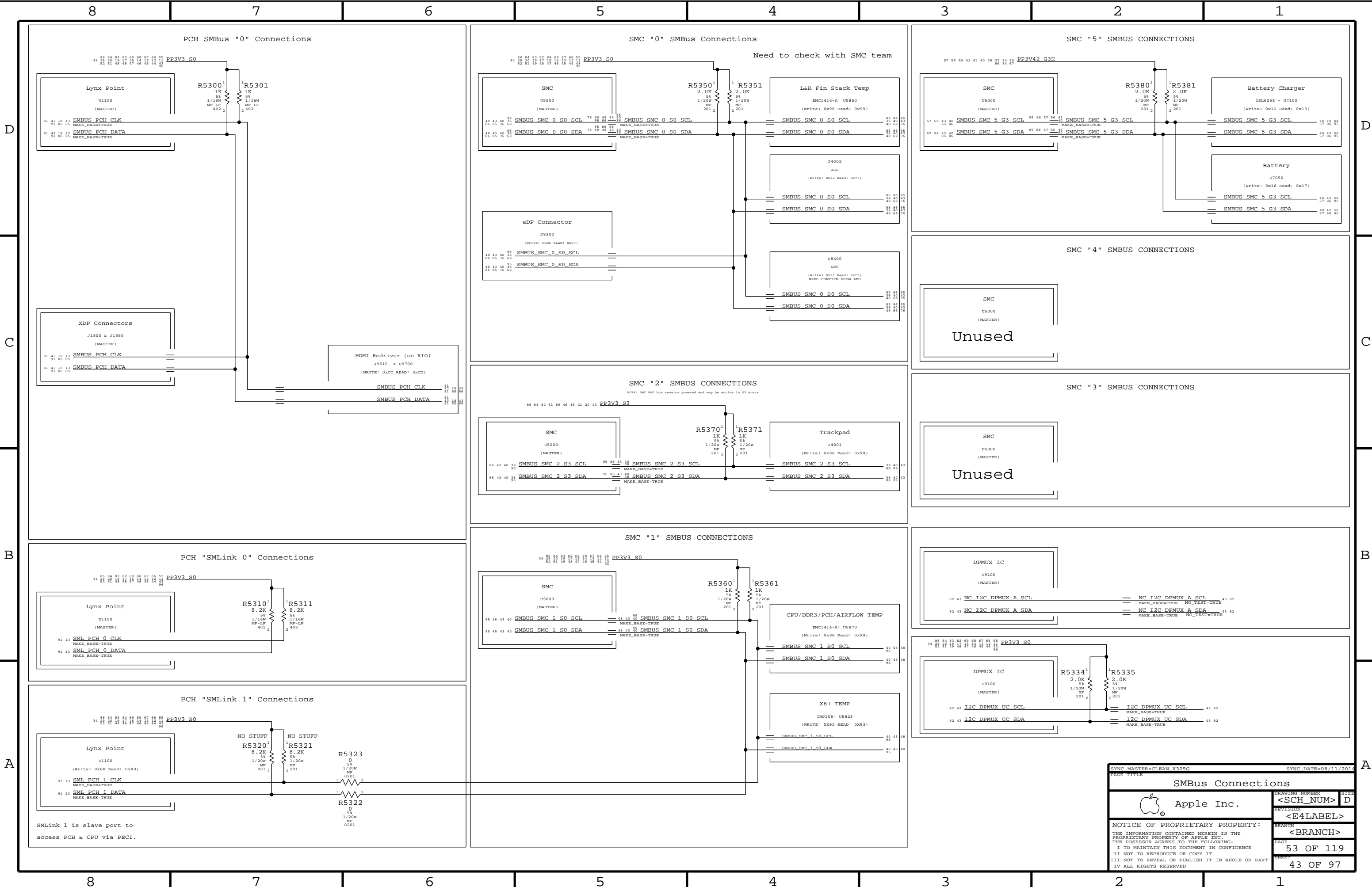
APN: 998-3029
OMIT_TABLE
J5250
HALL-SENSOR-MLB-PADS-K99

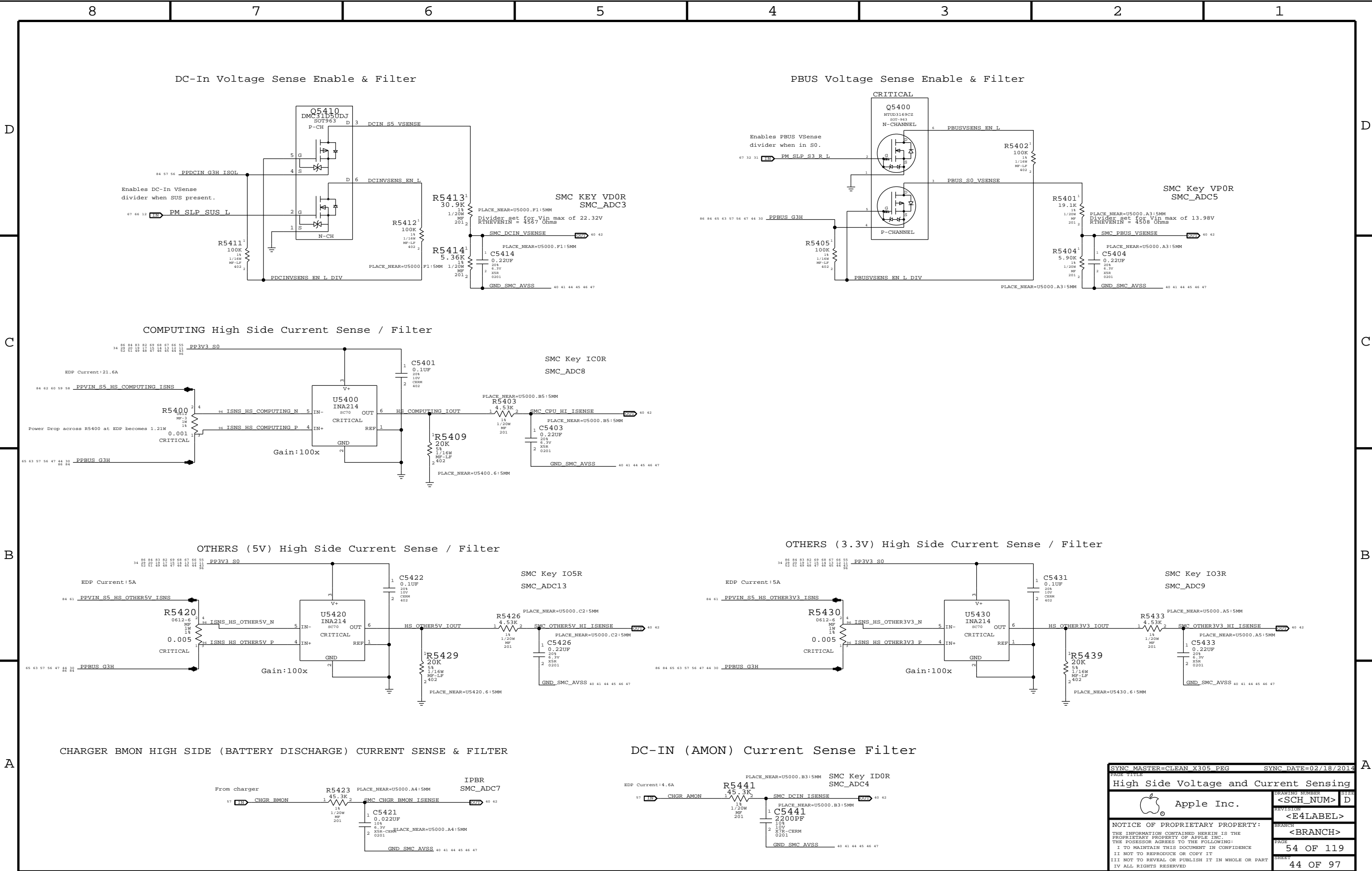



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6811	1	SUBASSY,PCBA HALL EFFECT,K99	J5250	CRITICAL	

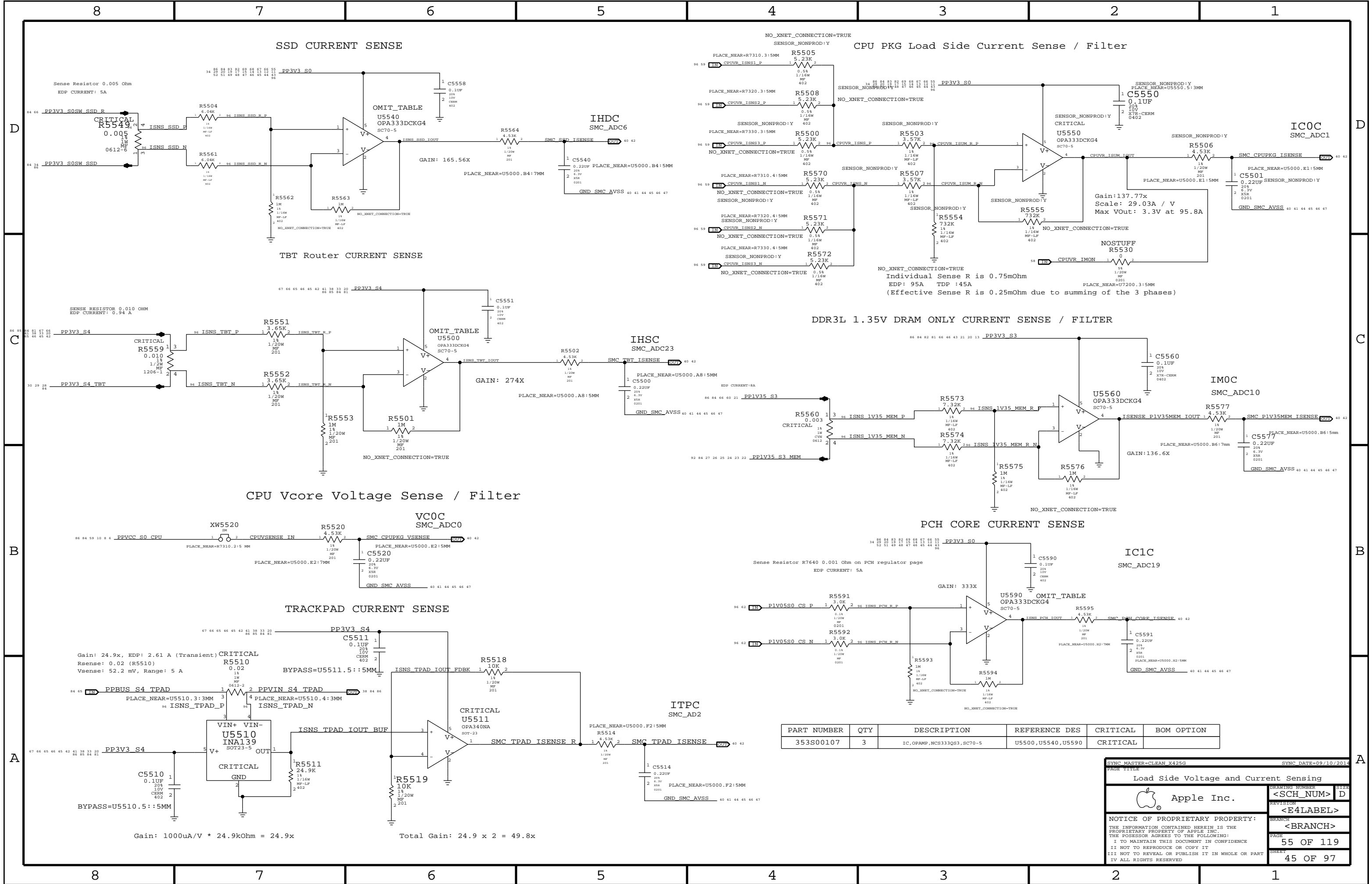


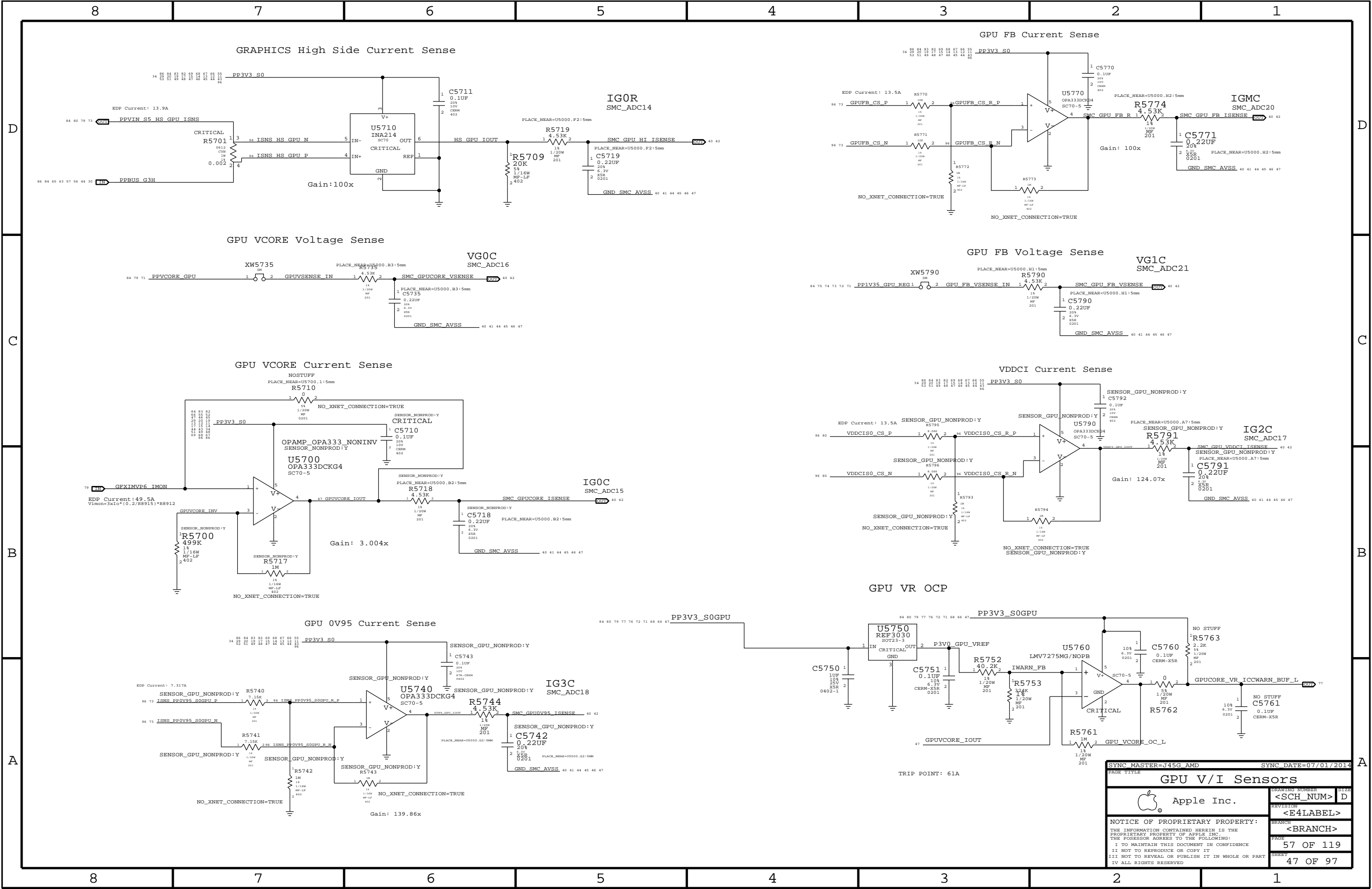
SMC Project Support	
Apple Inc.	DRAWING NUMBER <SCH_NUM>
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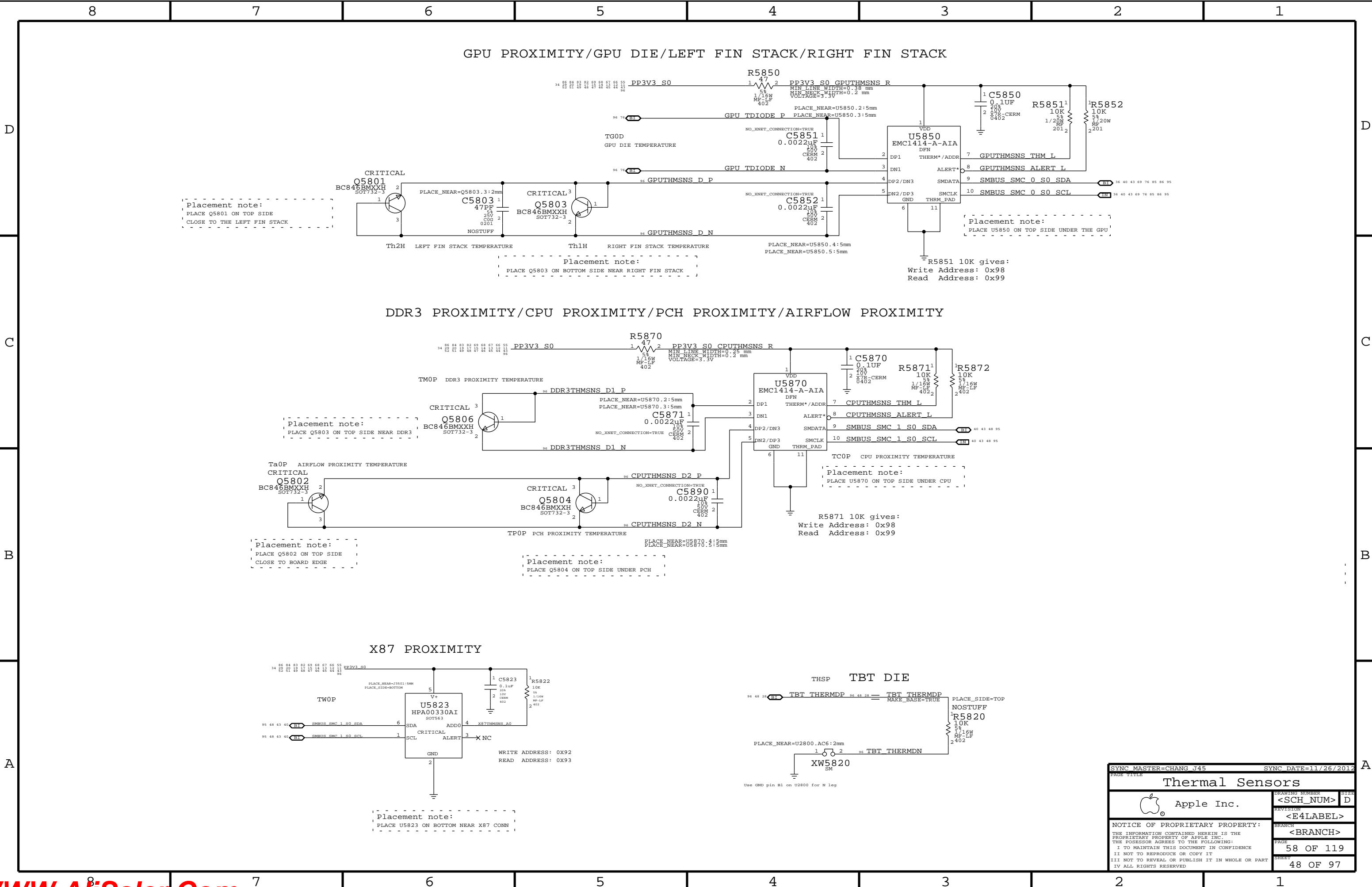




SYNC MASTER=CLEAN X305 PEG		SYNC DATE=02/18/2014	
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High Side Voltage and Current Sensing			
	DRAWING NUMBER		SIZE
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PAGE		54 OF 119	
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Placement note:
PLACE Q5801 ON TOP SIDE
CLOSE TO THE LEFT FIN STACK

Placement note:
PLACE Q5803 ON BOTTOM SIDE NEAR RIGHT FIN STACK

Placement note:
PLACE U5850 ON TOP SIDE UNDER THE GPU

R5851 10K gives:
Write Address: 0x98
Read Address: 0x99

Placement note:
PLACE Q5803 ON TOP SIDE NEAR DDR3

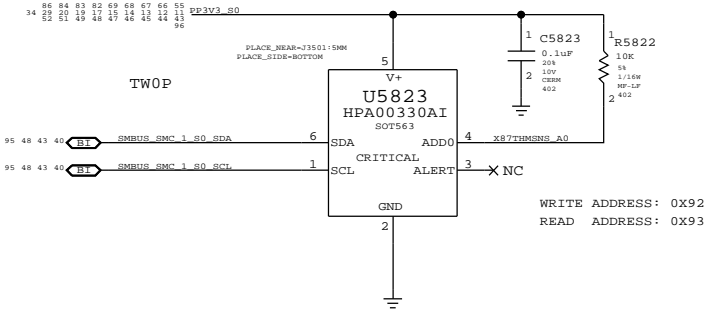
Placement note:
PLACE U5870 ON TOP SIDE UNDER CPU

R5871 10K gives:
Write Address: 0x98
Read Address: 0x99

Placement note:
PLACE Q5802 ON TOP SIDE
CLOSE TO BOARD EDGE

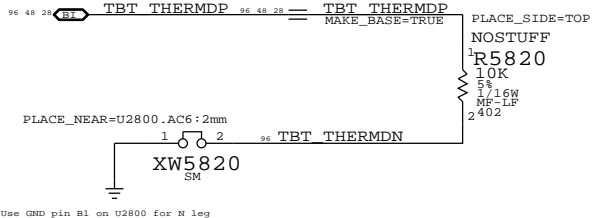
Placement note:
PLACE Q5804 ON TOP SIDE UNDER PCH

X87 PROXIMITY




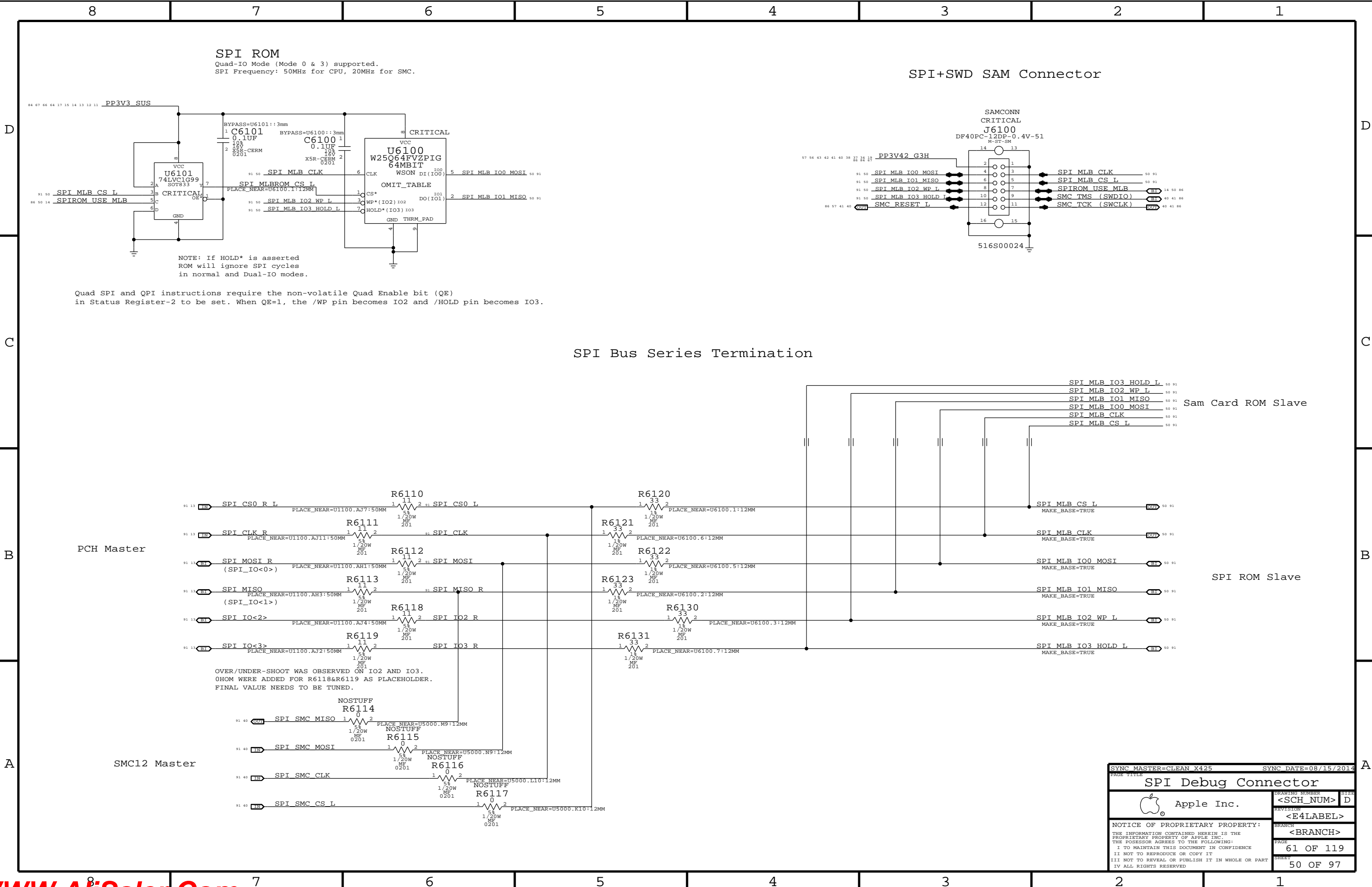
Placement note:
PLACE U5823 ON BOTTOM NEAR X87 CONN

TBT DIE



Use GND pin B1 on U2800 for N leg

SYNC MASTER=CHANG J45		SYNC DATE=11/26/2012	
PAGE TITLE			
Thermal Sensors			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
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SPI ROM
Quad-I/O Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.

SPI+SWD SAM Connector

NOTE: If HOLD* is asserted
ROM will ignore SPI cycles
in normal and Dual-I/O modes.

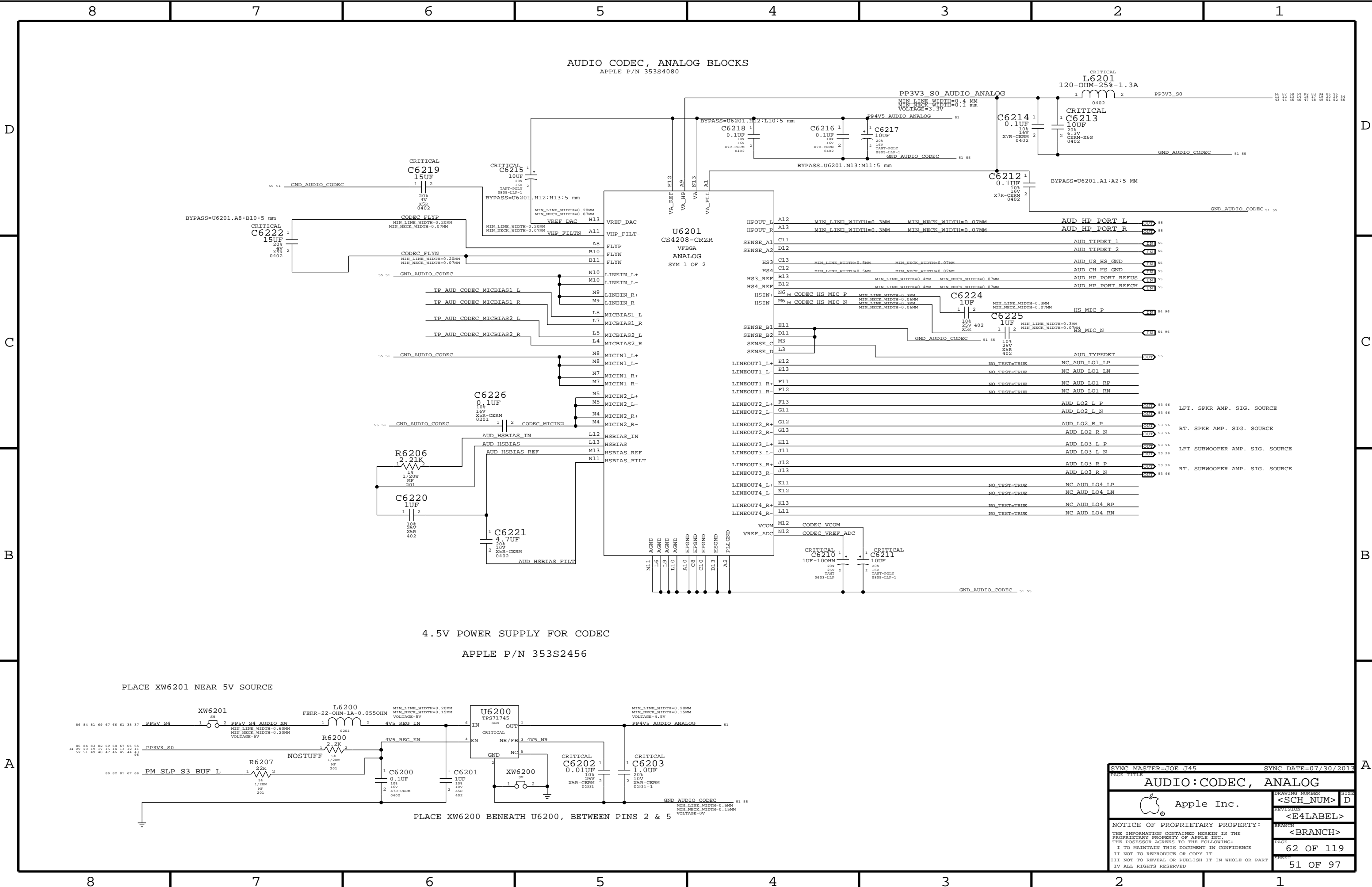
Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE)
in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.


SPI Bus Series Termination

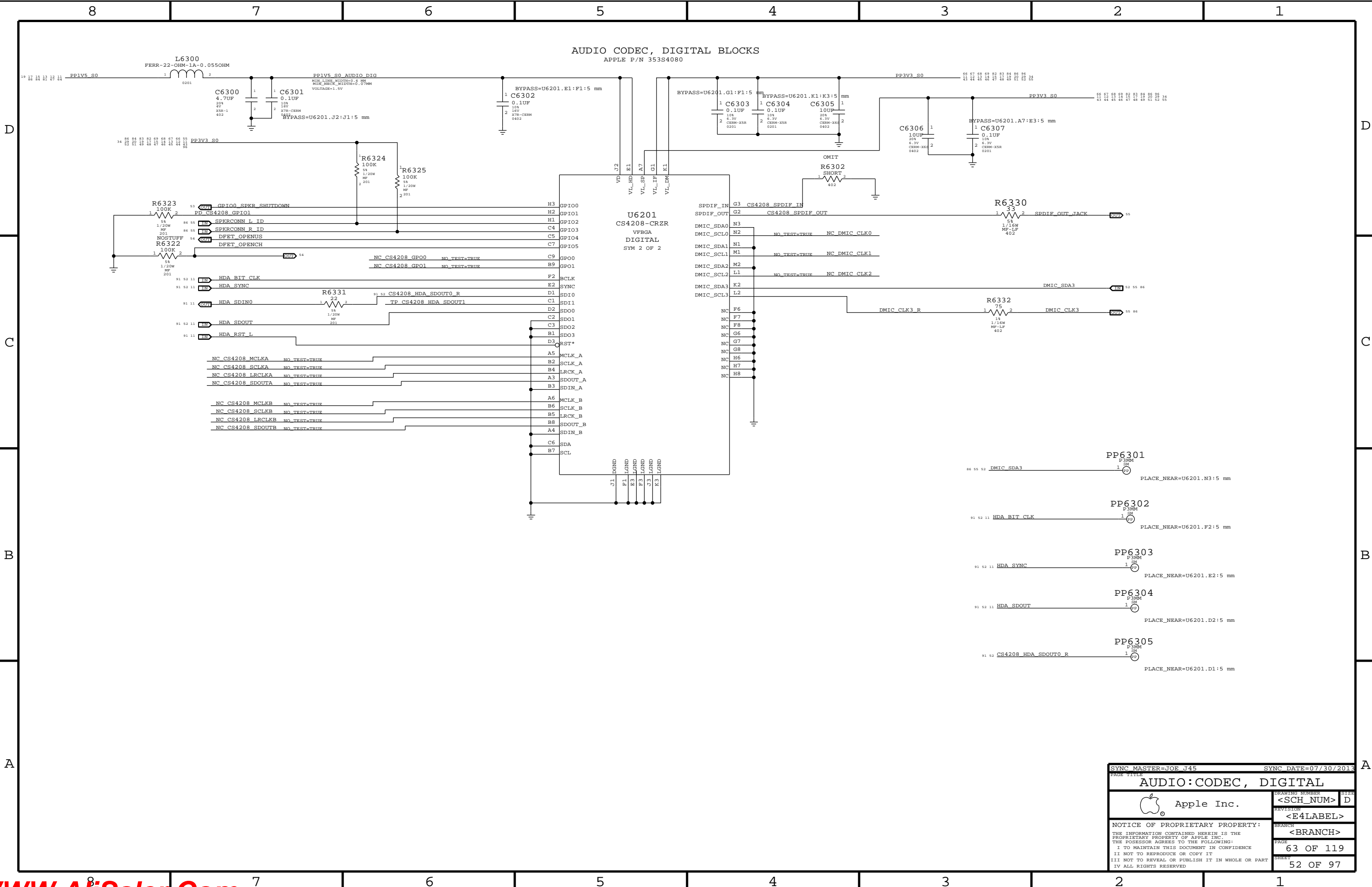
Sam Card ROM Slave


SPI ROM Slave

PAGE TITLE		SYNC MASTER=CLEAN X425		SYNC DATE=08/15/2014	
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Apple Inc.		<SCH_NUM>		D	
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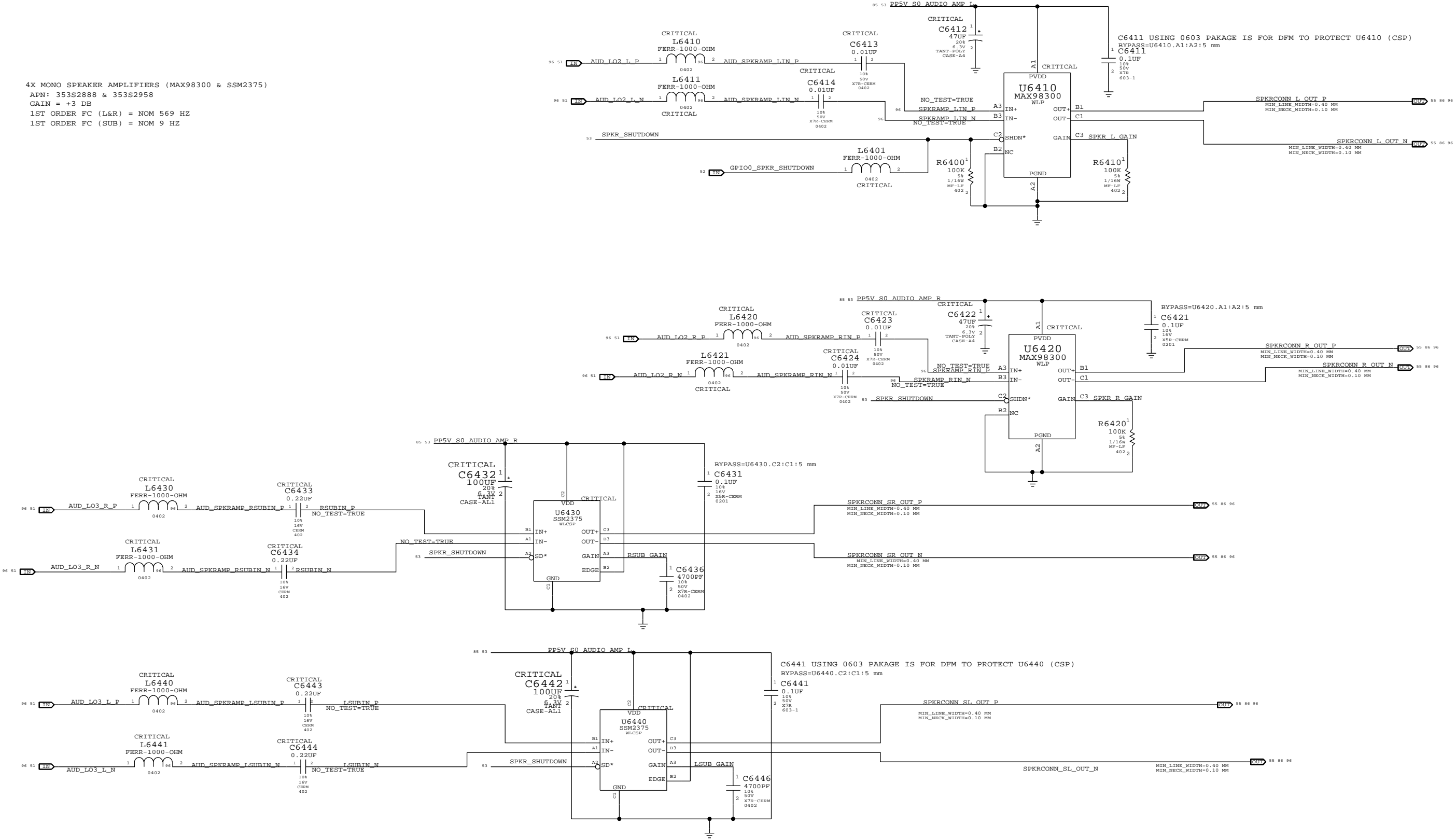



SYNC MASTER=JOE J45		SYNC DATE=07/30/2013	
PAGE TITLE			
AUDIO:CODEC, ANALOG			
 Apple Inc.	DRAWING NUMBER		SIZE
	<SCH_NUM>		D
	REVISED FOR		
	<E4LABEL>		
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BRANCH		<BRANCH>	
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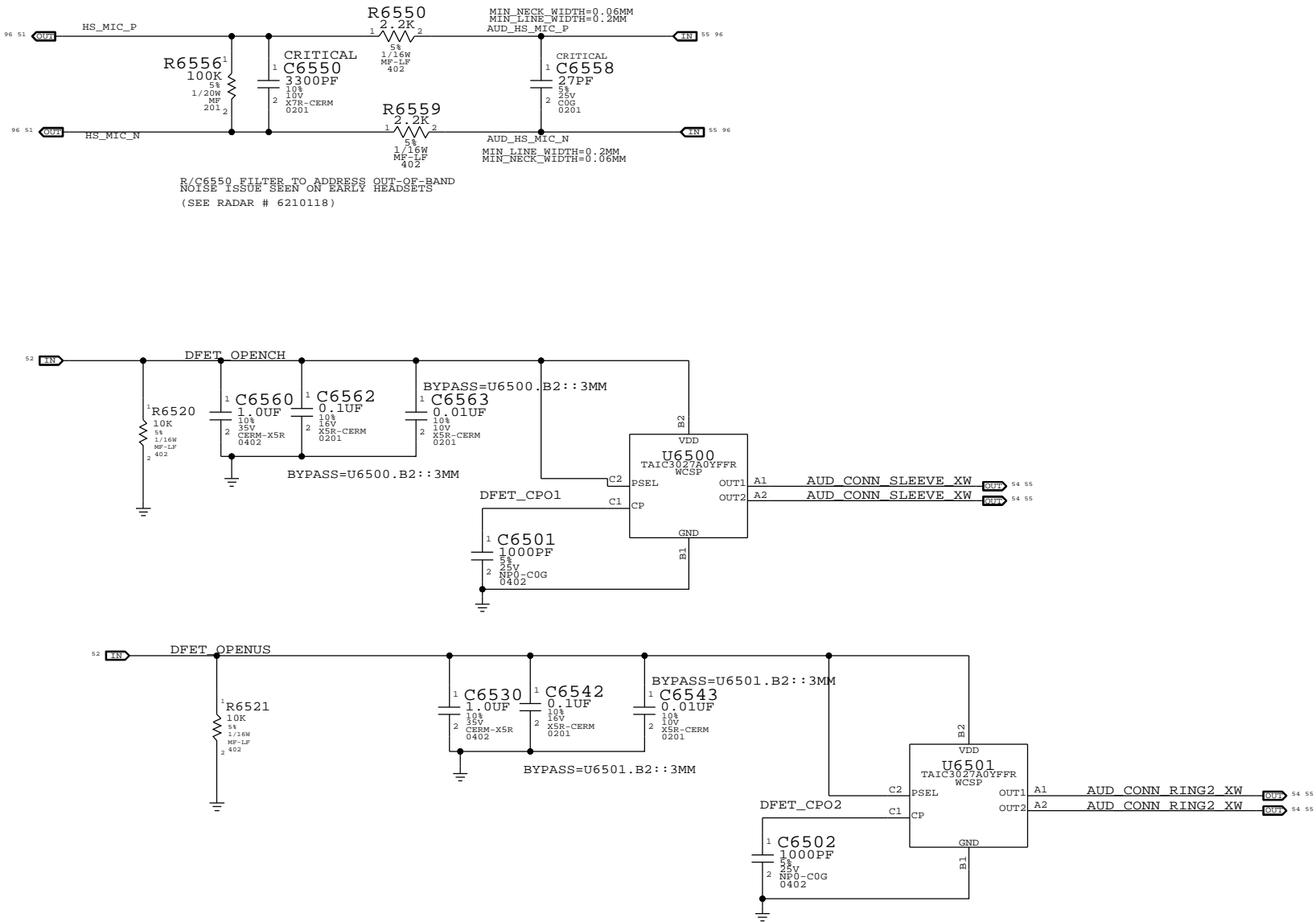



SYNC MASTER=JOE J45		SYNC DATE=07/30/2013	
PAGE TITLE			
AUDIO:CODEC, DIGITAL			
 Apple Inc.		DRAWING NUMBER	SIZE
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		BRANCH	
		<BRANCH>	
		PAGE	63 OF 119
		SHEET	52 OF 97

4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ

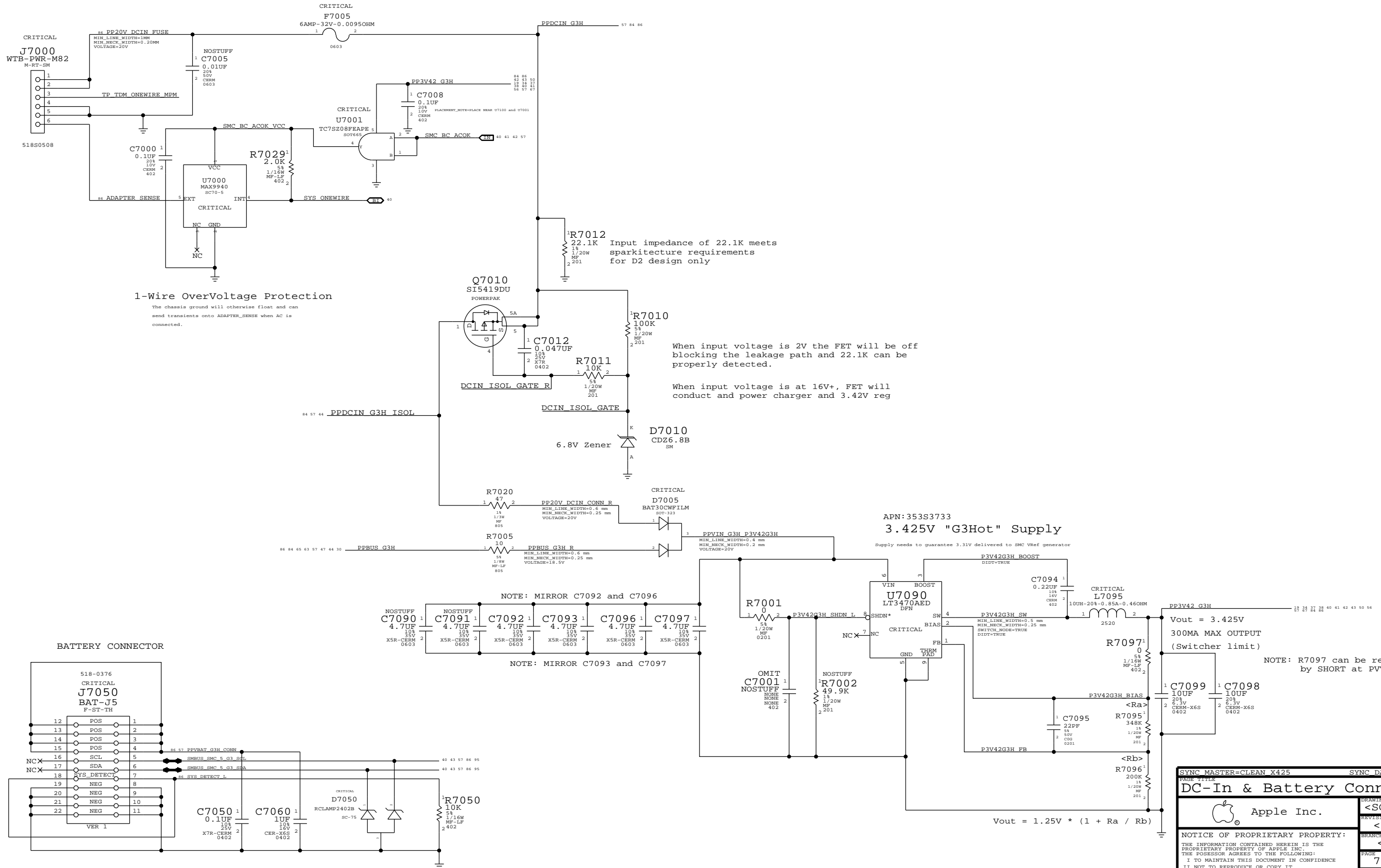


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PAGE TITLE			
AUDIO: SPEAKER AMP			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
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		PAGE	64 OF 119
		SHEET	53 OF 97

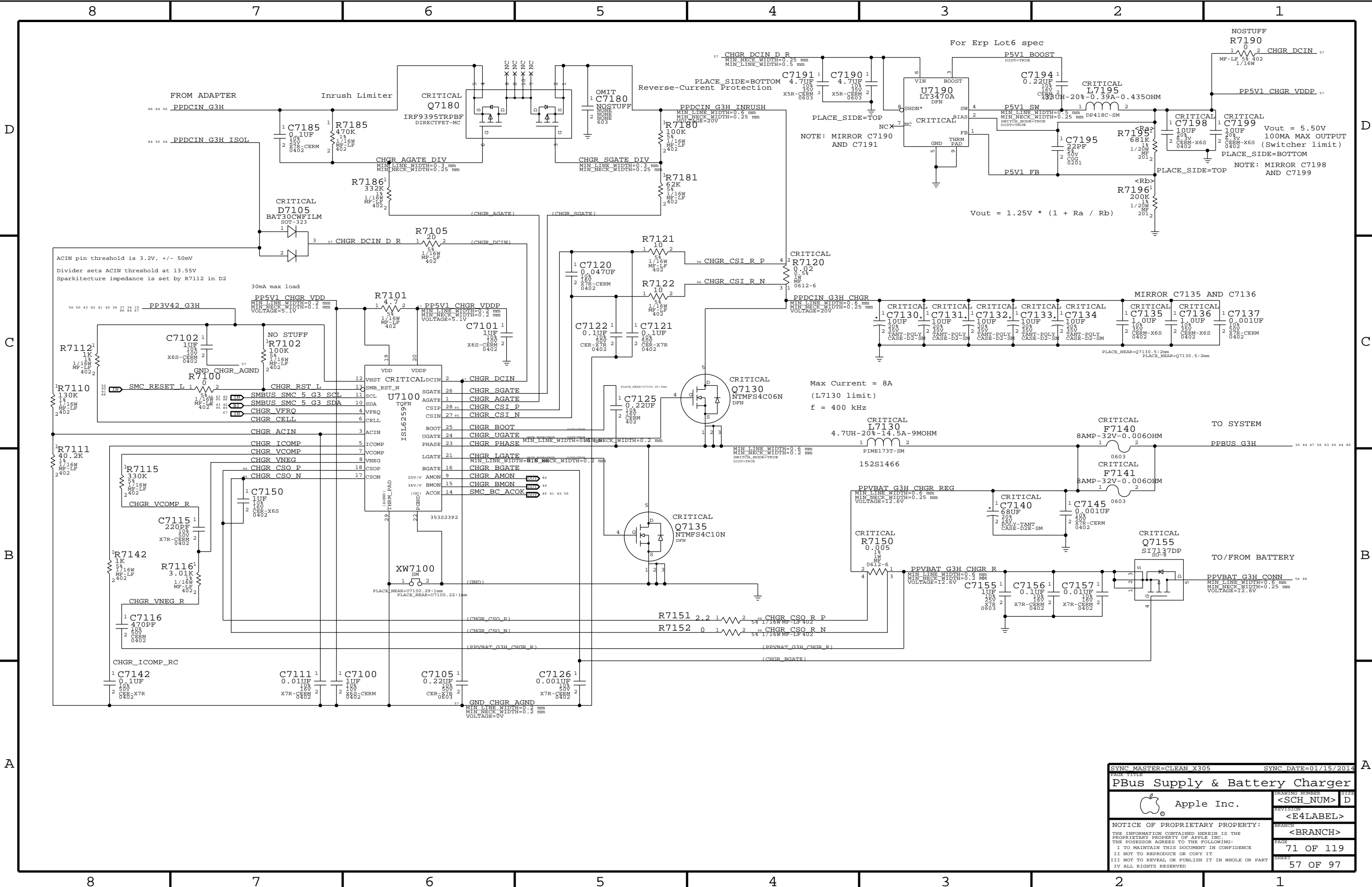


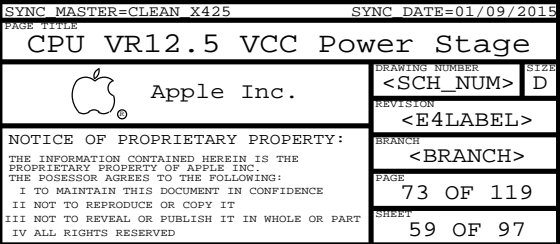
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PAGE TITLE			
AUDIO: JACK			
 Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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		SHEET	54 OF 97

MagSafe DC Power Jack



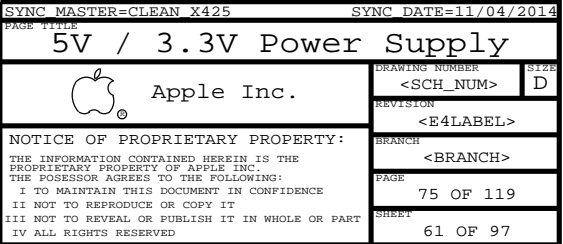
PAGE TITLE		SYNC MASTER=CLEAN X425		SYNC DATE=11/04/2014	
DC-In & Battery Connectors					
DRAWING NUMBER		SIZE		REVISION	
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REVISED		BRANCH		PAGE	
<BRANCH>		<BRANCH>		70 OF 119	
SHEET		SHEET		56 OF 97	
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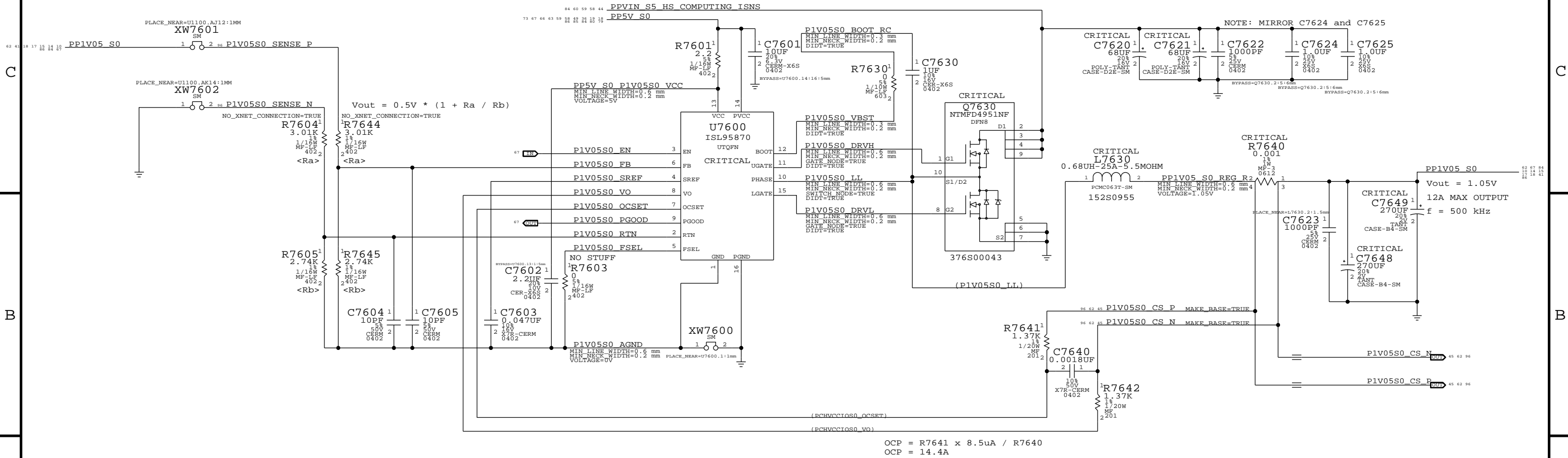


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A



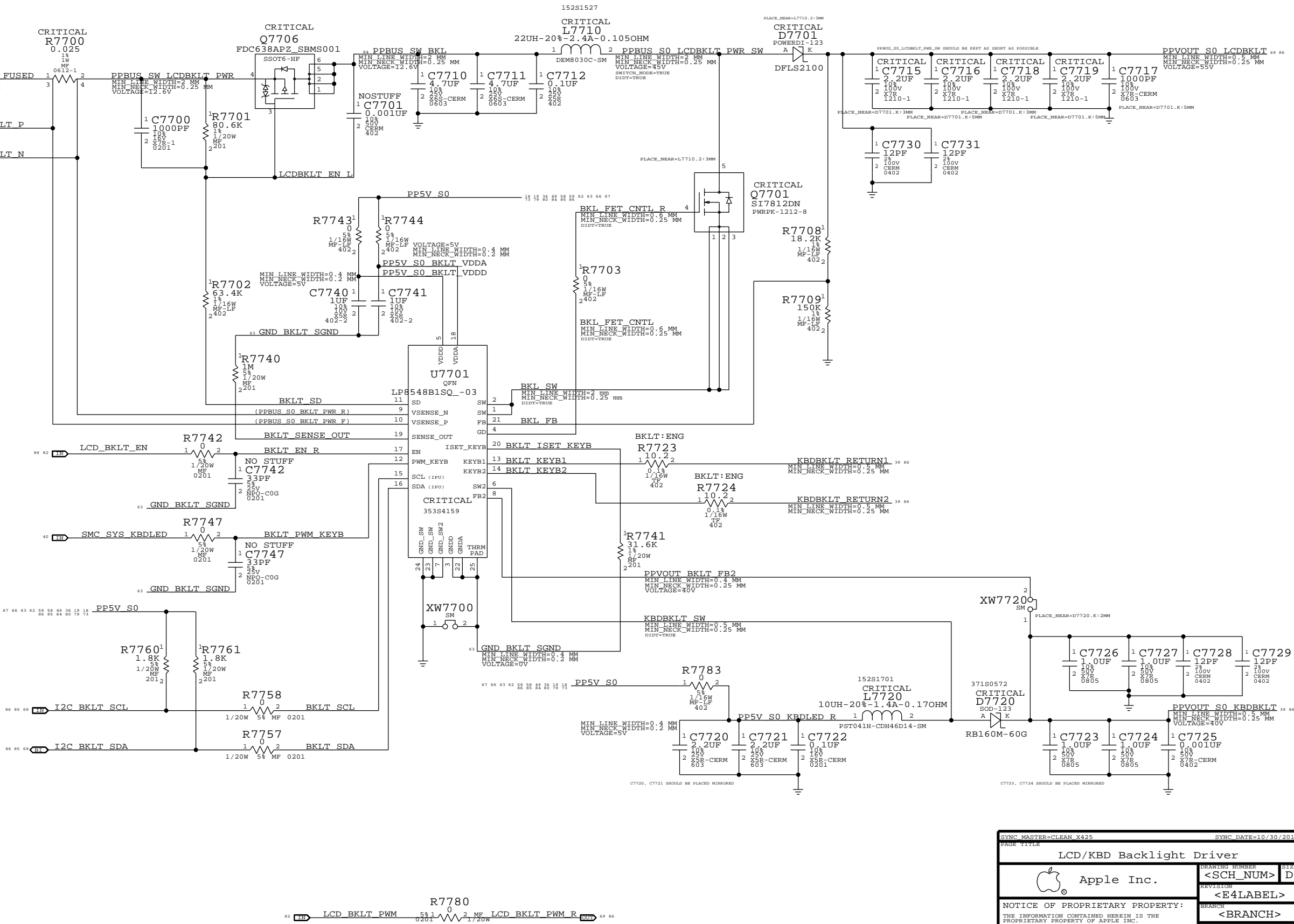
1V05 S0 REGULATOR




OCF = R7641 x 8.5uA / R7640
OCF = 14.4A

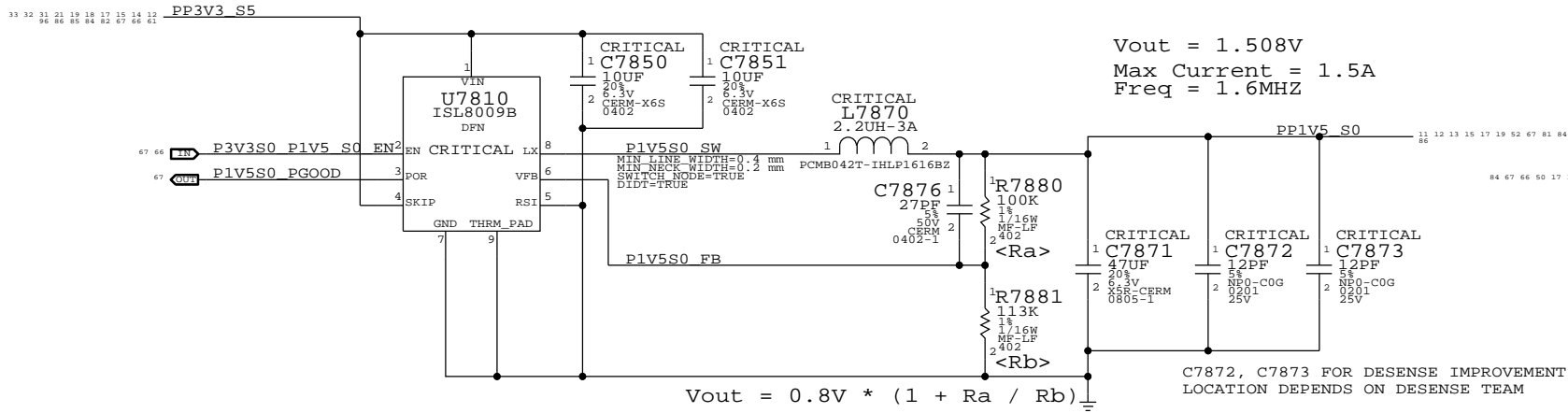
SYNC MASTER=CLEAN X305 PEG		SYNC DATE=02/18/2014	
PAGE TITLE			
1V05V POWER SUPPLY			
 Apple Inc.	DRAWING NUMBER	SIZE	
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7723,R7724		BKLT:PROD



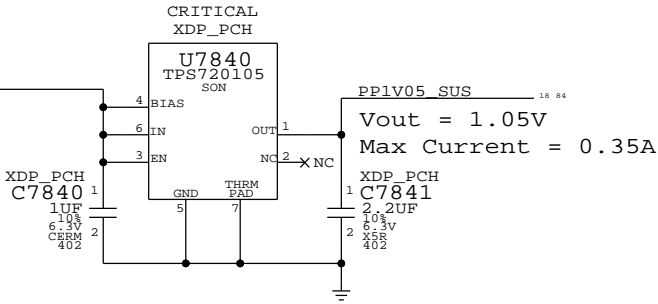
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PAGE TITLE			
LCD/KBD Backlight Driver			
	Apple Inc.		DRAWING NUMBER <SCH_NUM>
			SIZE D
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
1.5V S0 Regulator

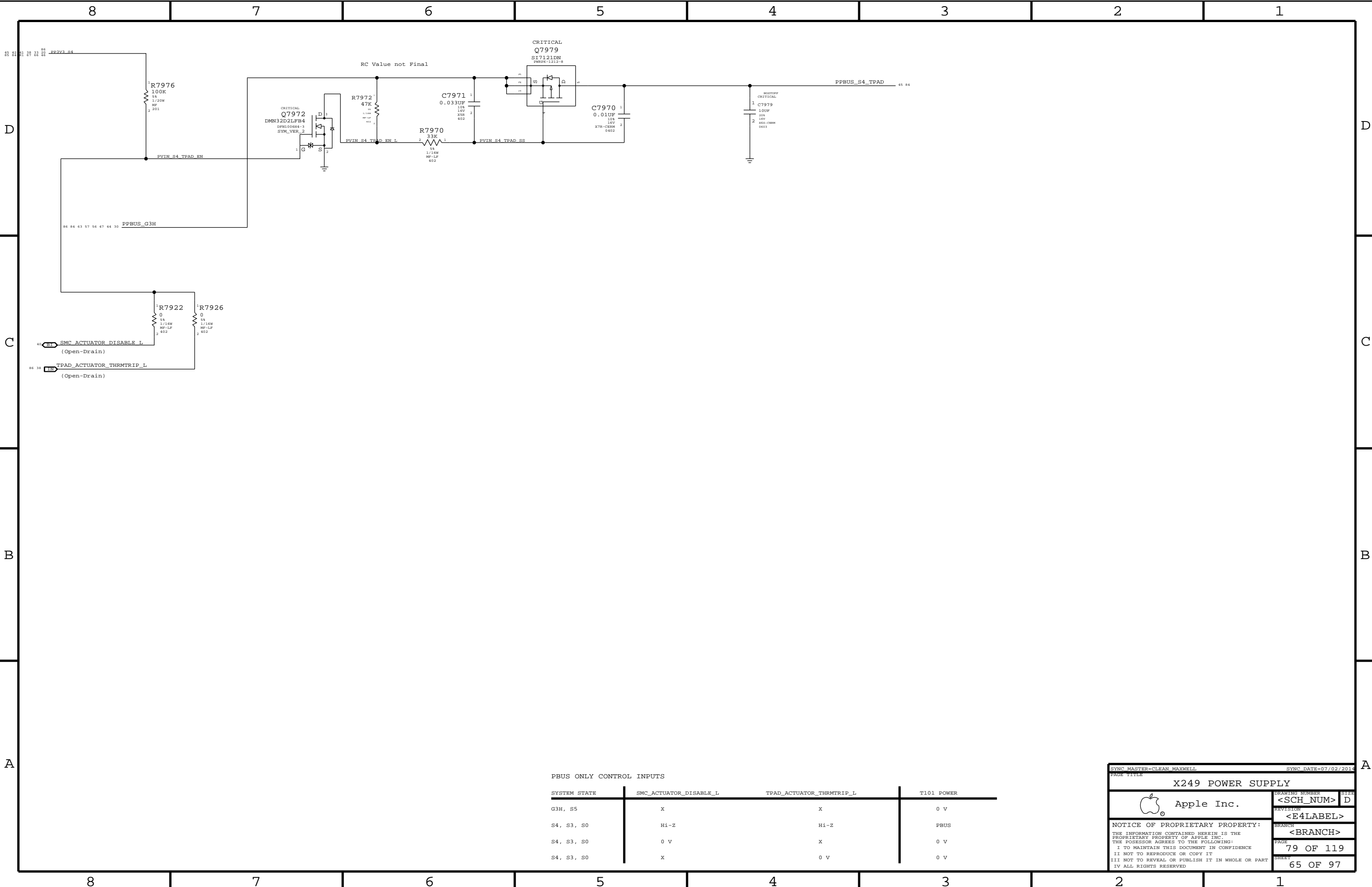


1.05V SUS LDO

Lynx Point-H requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V SUS, which burns 100mW in all S-states.



SYNC MASTER=CLEAN X305		SYNC DATE=01/15/2014	
PAGE TITLE			
Misc Power Supplies		DRAWING NUMBER	
	Apple Inc.	<SCH_NUM>	D
		REVISION	
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		BRANCH	
		<BRANCH>	
		PAGE	78 OF 119
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PBUS ONLY CONTROL INPUTS

SYSTEM STATE	SMC_ACTUATOR_DISABLE_L	TPAD_ACTUATOR_THRMTRIP_L	T101 POWER
G3H, S5	X	X	0 V
S4, S3, S0	Hi-Z	Hi-Z	PBUS
S4, S3, S0	0 V	X	0 V
S4, S3, S0	X	0 V	0 V

SYNC MASTER=CLEAN MAXWELL

SYNC DATE=07/02/2014

X249 POWER SUPPLY

 Apple Inc.

DRAWING NUMBER

<SCH_NUM>

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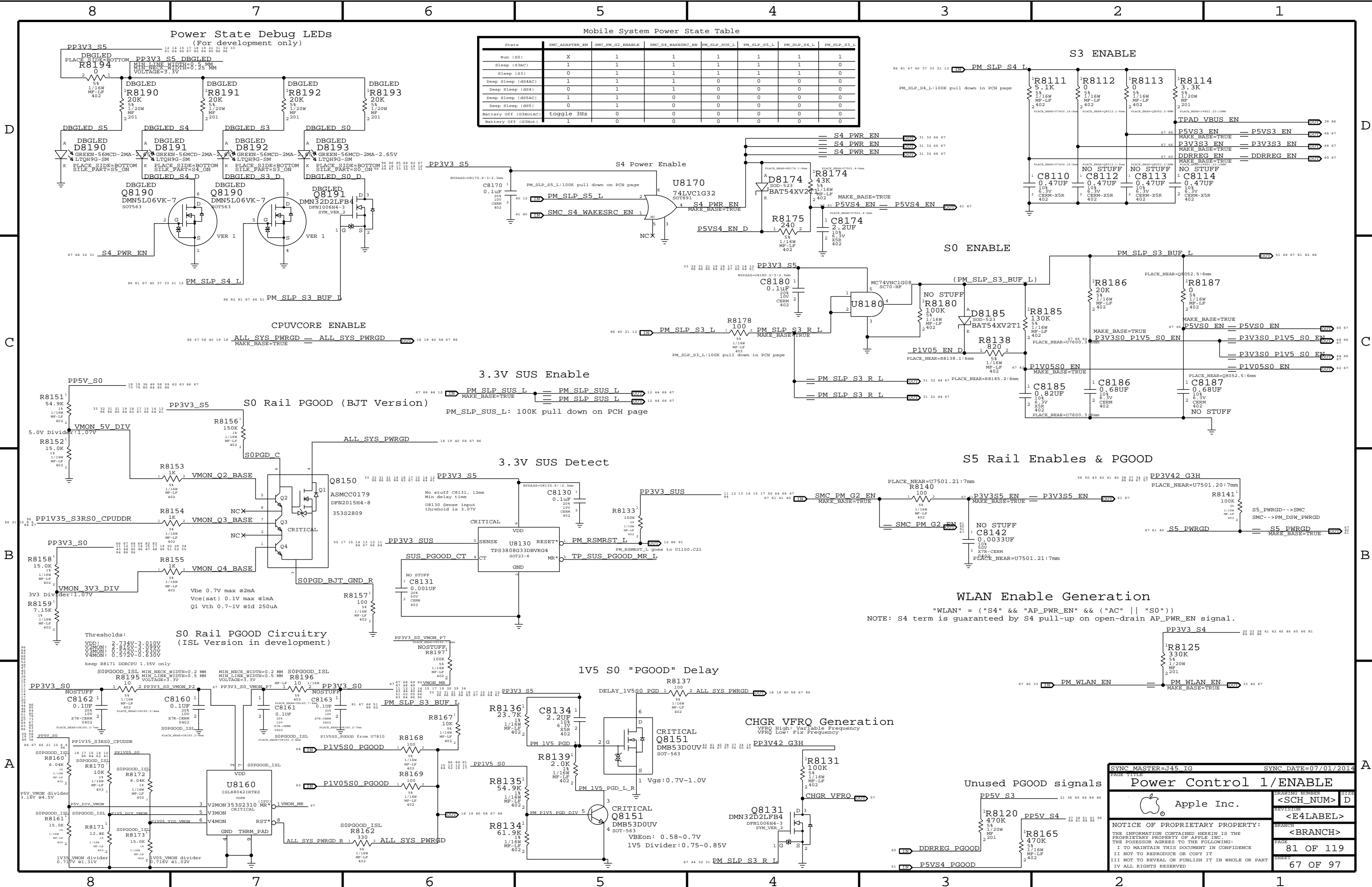
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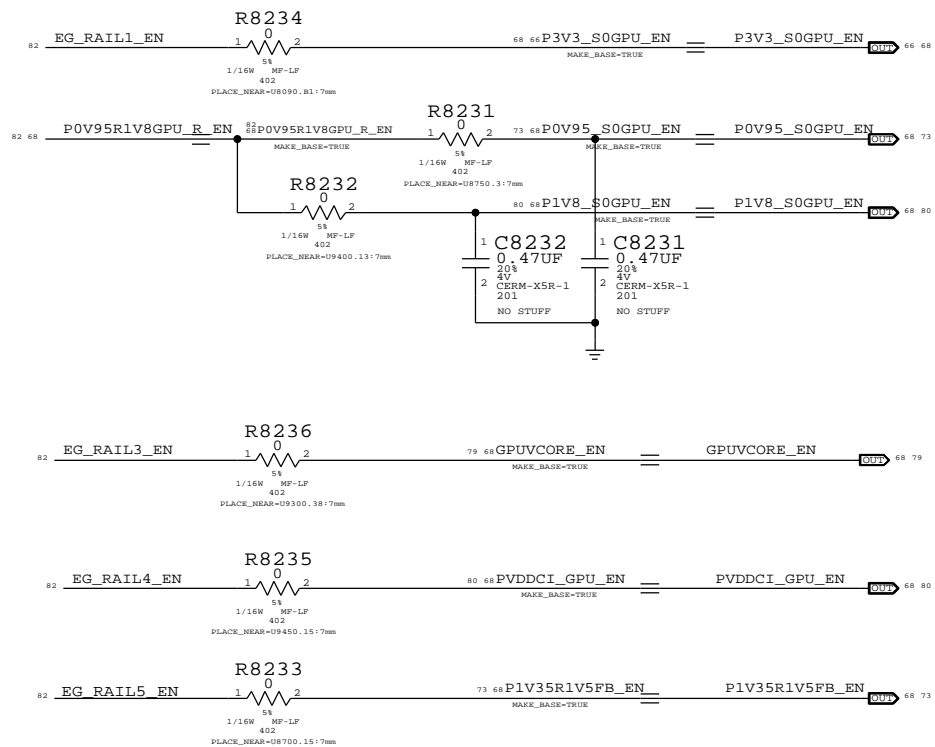
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SYNC DATE=07/01/2014

Power Control 1/ENABLE		DRAWING NUMBER	SIZE
Apple Inc.		<SCH_NUM>	D
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Venus GPU requires rails to come up in the following order:

- 1) GPU_3.3V
- 2) GPU_0V95 (BIF_VDDC) & GPU_1V8 (VDD_CT)
- 3) GPUVCORE
- 4) VDDCI
- 5) FB VRAM MVDD



84 80 79 77 76 72 71 66 47 PP3V3 S0GPU

R8290¹ 100K 5% 1/20W MF 201 2

R8291¹ 100K 5% 1/20W MF 201 2

R8292¹ 100K 5% 1/20W MF 201 2

R8293¹ 100K 5% 1/20W MF 201 2

R8294¹ 100K 5% 1/20W MF 201 2

R8296¹ 10K 5% 1/20W MF 201 2

82 79 68 GPUVCORE_PGOOD MAKE_BASS=TRUE

73 68 P1V35R1V5FB_PGOOD

82 73 68 P0V95_S0GPU_PGOOD MAKE_BASS=TRUE

82 80 68 PVDDCI_PGOOD MAKE_BASS=TRUE

82 80 68 P1V8GPU_PGOOD MAKE_BASS=TRUE

82 68 P3V3_S0GPU_PGOOD MAKE_BASS=TRUE

68 79 82 GPUVCORE_PGOOD

68 73 P1V35R1V5FB_PGOOD 73

68 73 82 P0V95_S0GPU_PGOOD

68 80 82 PVDDCI_PGOOD

68 80 82 P1V8GPU_PGOOD

68 82 P3V3_S0GPU_PGOOD

PGOOD ON SEQUENCE

1. GPU 3V3 GPU_PGGOOD1
2. 0.95_S0GPU GPU_PGGOOD6_2
3. 1V8_GPU GPU_PGGOOD2
4. GPUVCORE GPU_PGGOOD3
5. VDDCI GPU_PGGOOD4
6. FB MVDD GPU_PGGOOD5

(GPU_PGGOOD6_2 is up before 1V8GPU_PGOOD after 3V3GPU_PGGOOD)

R8295

73 68 P1V35R1V5FB_PGOOD 1 0 2 PM_ALL_GPU_PGOOD

5% 1/20W MF 201 2

68 82

```

GND_Void=TRUE
PLACE_HEAR=C8420.1:3mm
C8220
0.22UF
PEG_D2R_C_P<0>
1 2
20%
6.3V
X5R
201
NOSTUFF
GAP_PEG_D2R_P0
PLACE_HEAR=C8420.1:3mm
R8220
49.9
1%
1/20W
MF
201
NOSTUFF
GND_Void=TRUE
PLACE_HEAR=C8421.1:3mm
C8221
0.22UF
PEG_D2R_C_N<0>
1 2
20%
6.3V
X5R
201
NOSTUFF
GAP_PEG_D2R_N0
PLACE_HEAR=C8421.1:3mm
R8221
49.9
1%
1/20W
MF
201
NOSTUFF
GND_Void=TRUE
PLACE_HEAR=C8434.1:3mm
C8240
0.22UF
PEG_R2D_C_P<0>
1 2
20%
6.3V
X5R
201
NOSTUFF
GAP_PEG_R2D_P0
PLACE_HEAR=C8434.1:3mm
R8240
49.9
1%
1/20W
MF
201
NOSTUFF
GND_Void=TRUE
PLACE_HEAR=C8435.1:3mm
C8241
0.22UF
PEG_R2D_C_N<0>
1 2
20%
6.3V
X5R
201
NOSTUFF
GAP_PEG_R2D_N0
PLACE_HEAR=C8435.1:3mm
R8241
49.9
1%
1/20W
MF
201
NOSTUFF

```

```

14      96 86 84 83 82 69 67 66
56 29 20 19 17 15 14 13 12 11
55 52 51 49 48 47 46 45 44 43

```

PP3V3_S0

DBGLED
R8212
20K
51
1/20W
MF
201


DBG_RAIL5_5

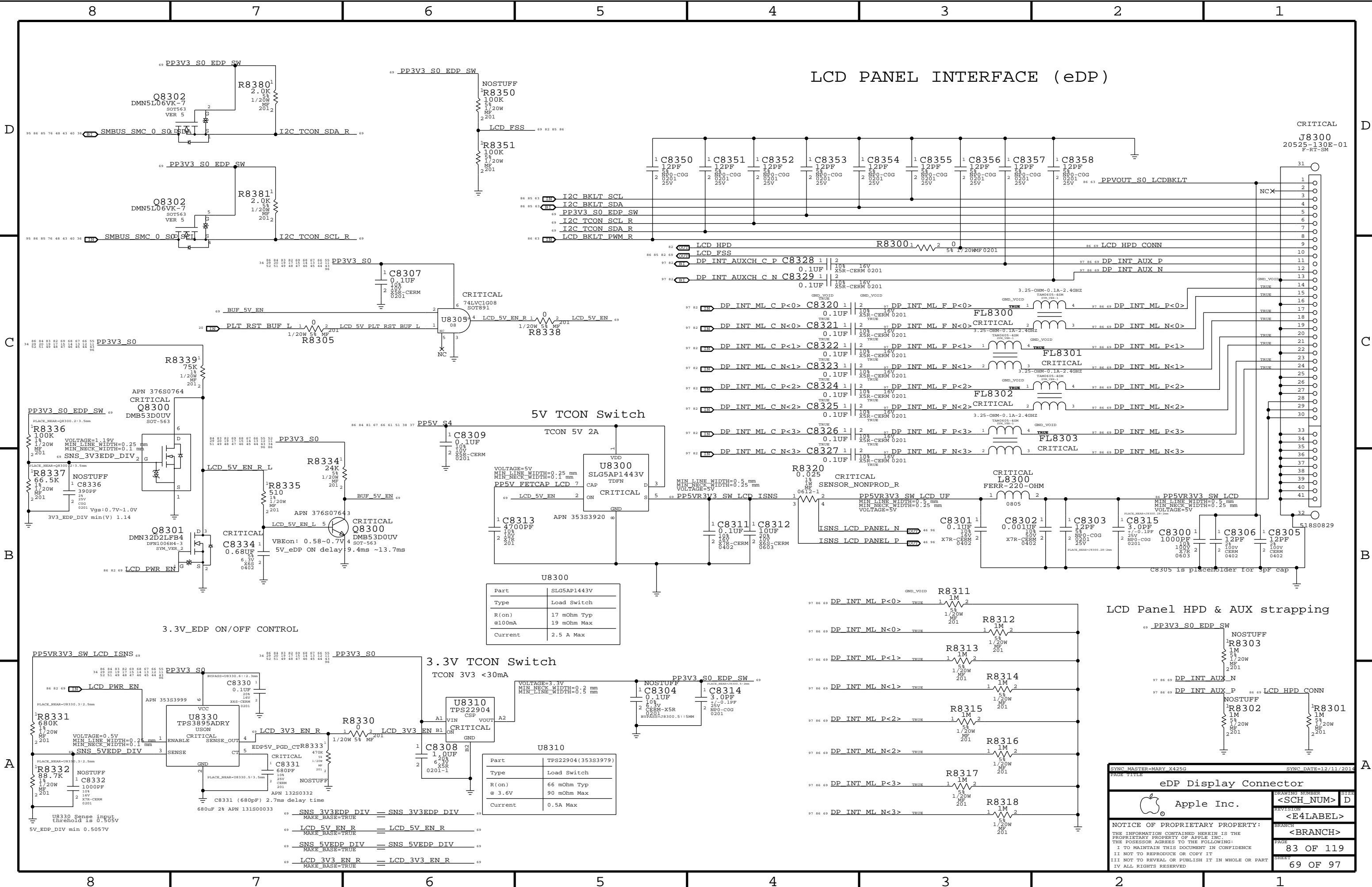
A
DBGLED
D8211
GREEN-56MCD-ZMA-2.65V
LTQH9G-SM
K
PLACE_SIDE=BOTTOM
SILK_PART=ALL_GPU_PGOOD
DBG_RAIL5_D

3
DBGLED
Q8210
DMN32D2LFB4
DFN1006H4-3
SYM_VER_1

1 G
2

82 68 PM_ALL_GPU_PGOOD

SYNC MASTER=MARY X425G		SYNC DATE=09/11/2014	
PAGE TITLE			
Power Sequencing EG/PGOOD			
	Apple Inc.		DRAWING NUMBER <SCH_NUM>
			SIZE D
		REVISION <E4LABEL>	
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Part	SLG5AP1443V
Type	Load Switch
R(on)	17 mOhm Typ
@100mA	19 mOhm Max
Current	2.5 A Max

Part	TPS22904(353S3979)
Type	Load Switch
R(on)	66 mOhm Typ
@ 3.6V	90 mOhm Max
Current	0.5A Max

SYNC MASTER=MARY X425G

SYNC DATE=12/11/2014

PAGE TITLE

eDP Display Connector

Apple Inc.

Apple Inc.

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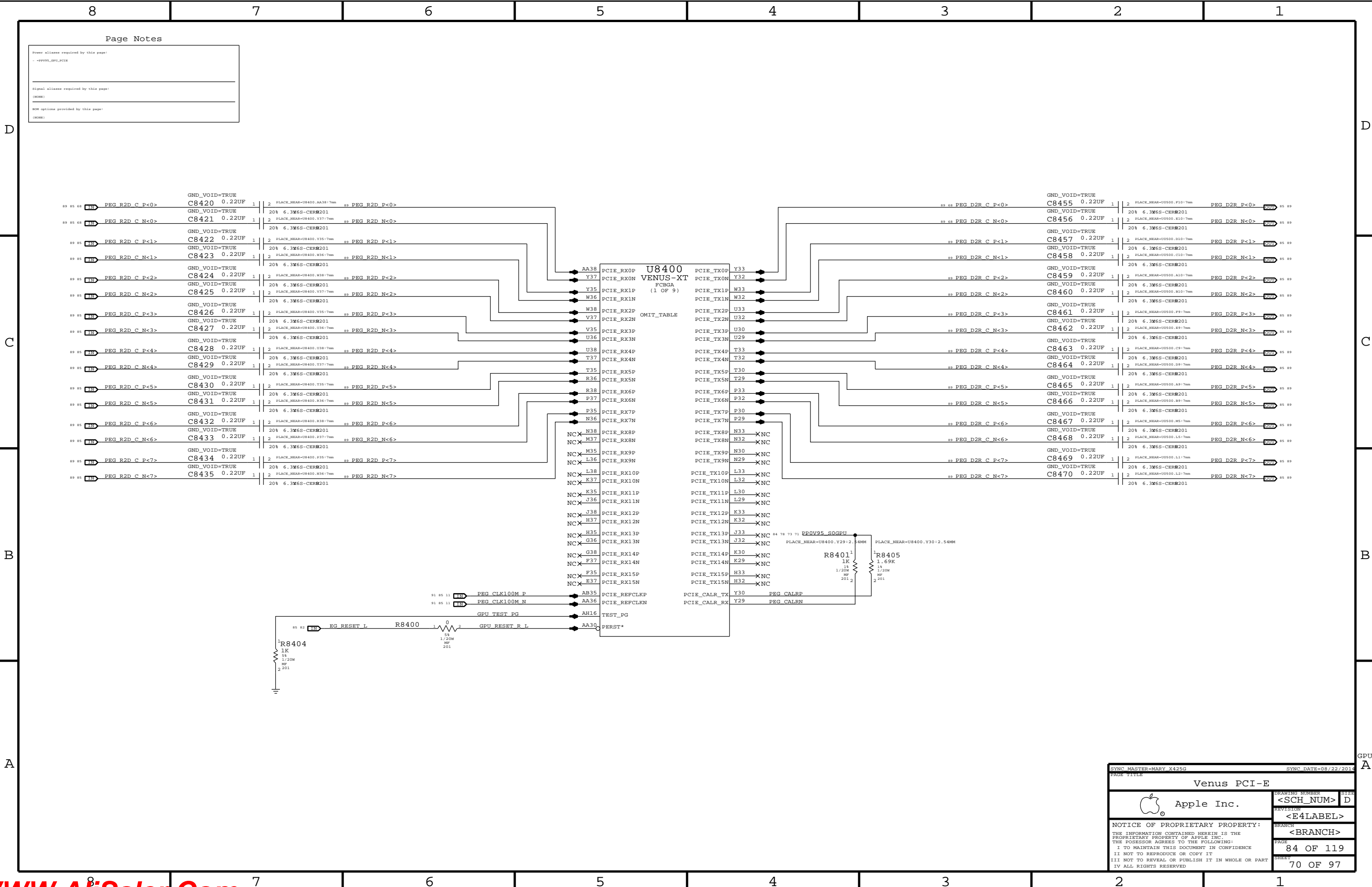
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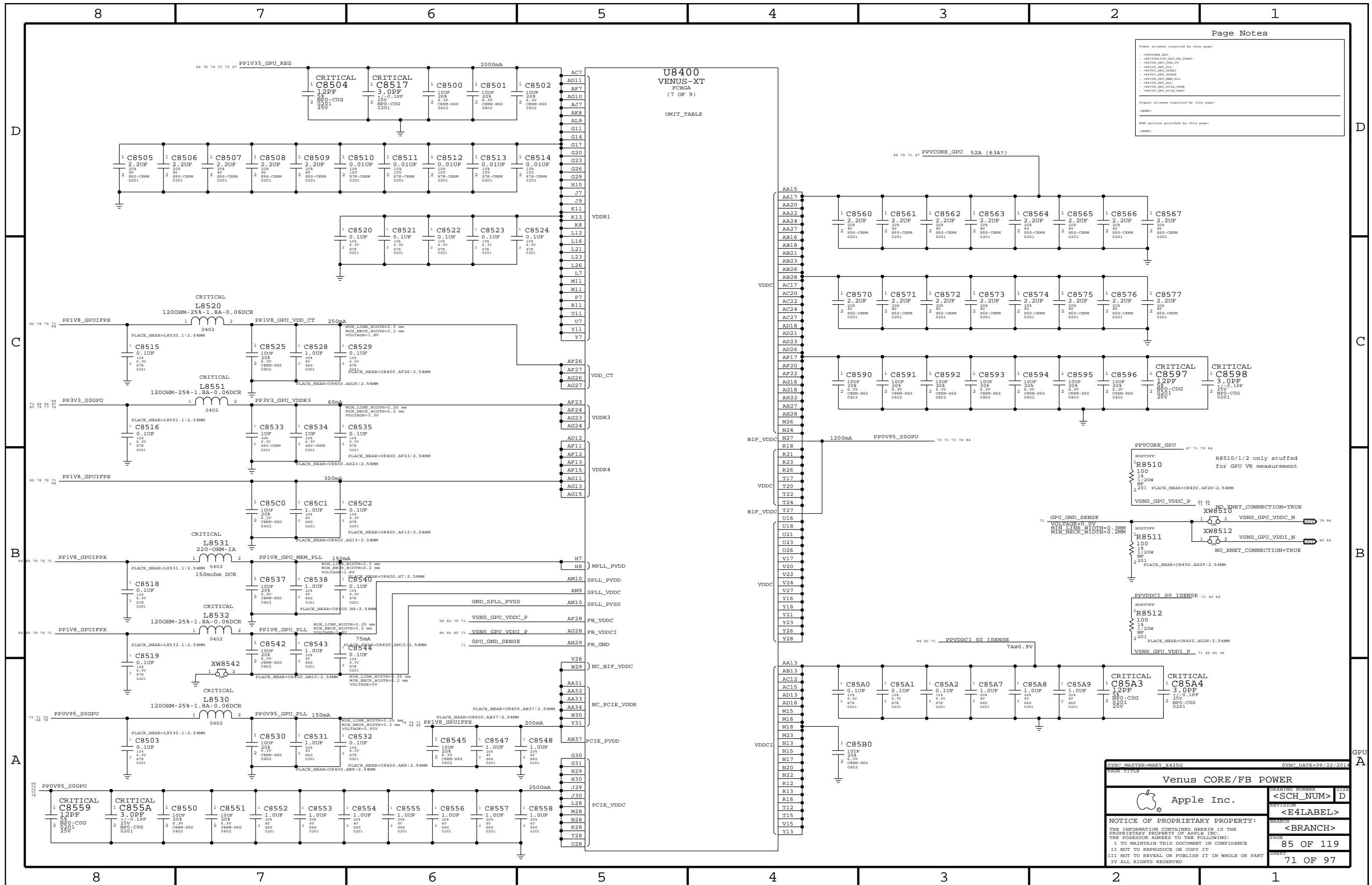
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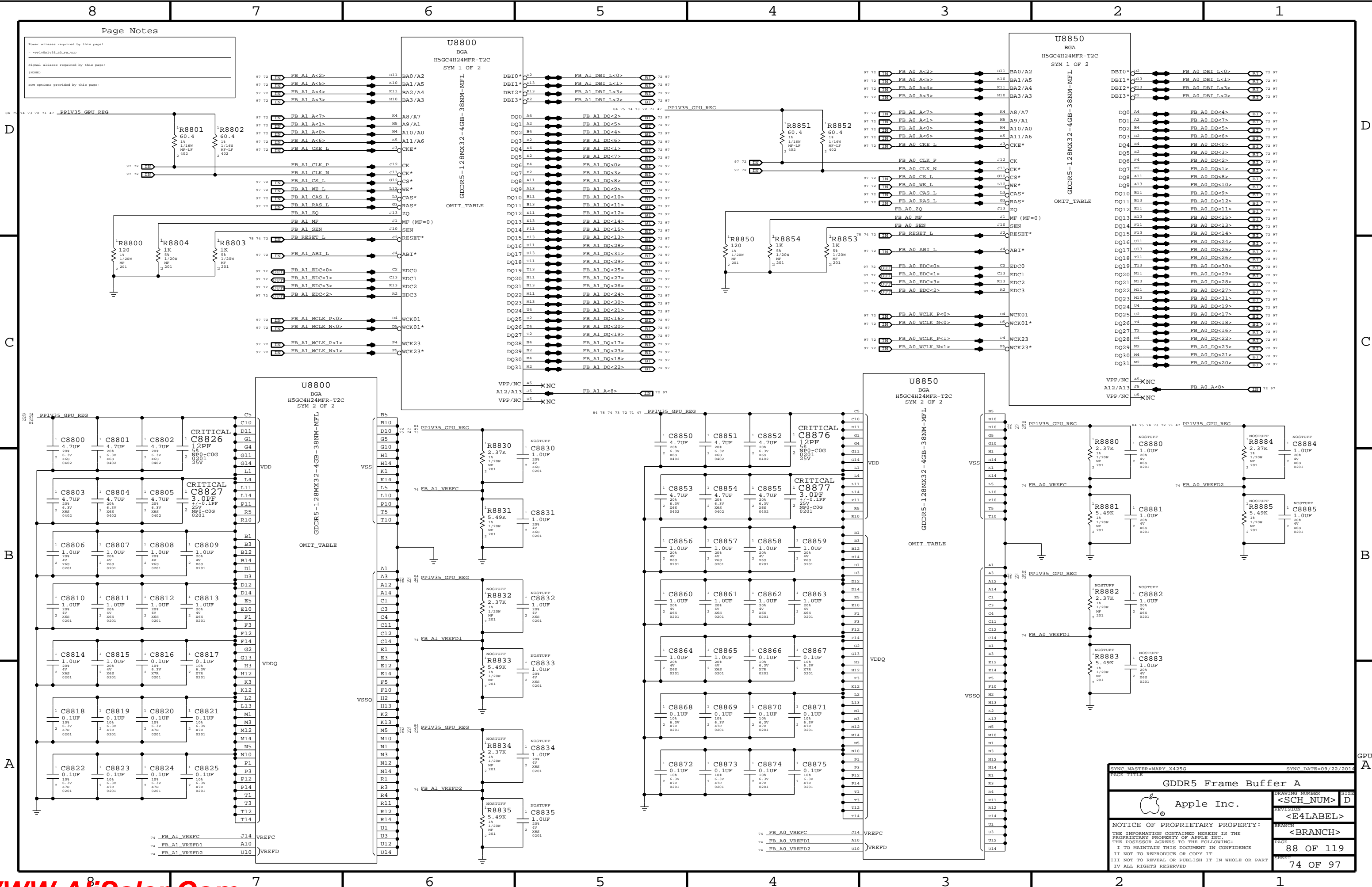
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-->P0V95_GPU_PCIE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC MASTER=MARY_X425G		SYNC DATE=08/22/2014	
PAGE TITLE			
Venus PCI-E			
	Apple Inc.	DRAWING NUMBER	SIZE
		<SCH_NUM>	D
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SYNC MASTER=MARY X425G

SYNC DATE=09/22/2014

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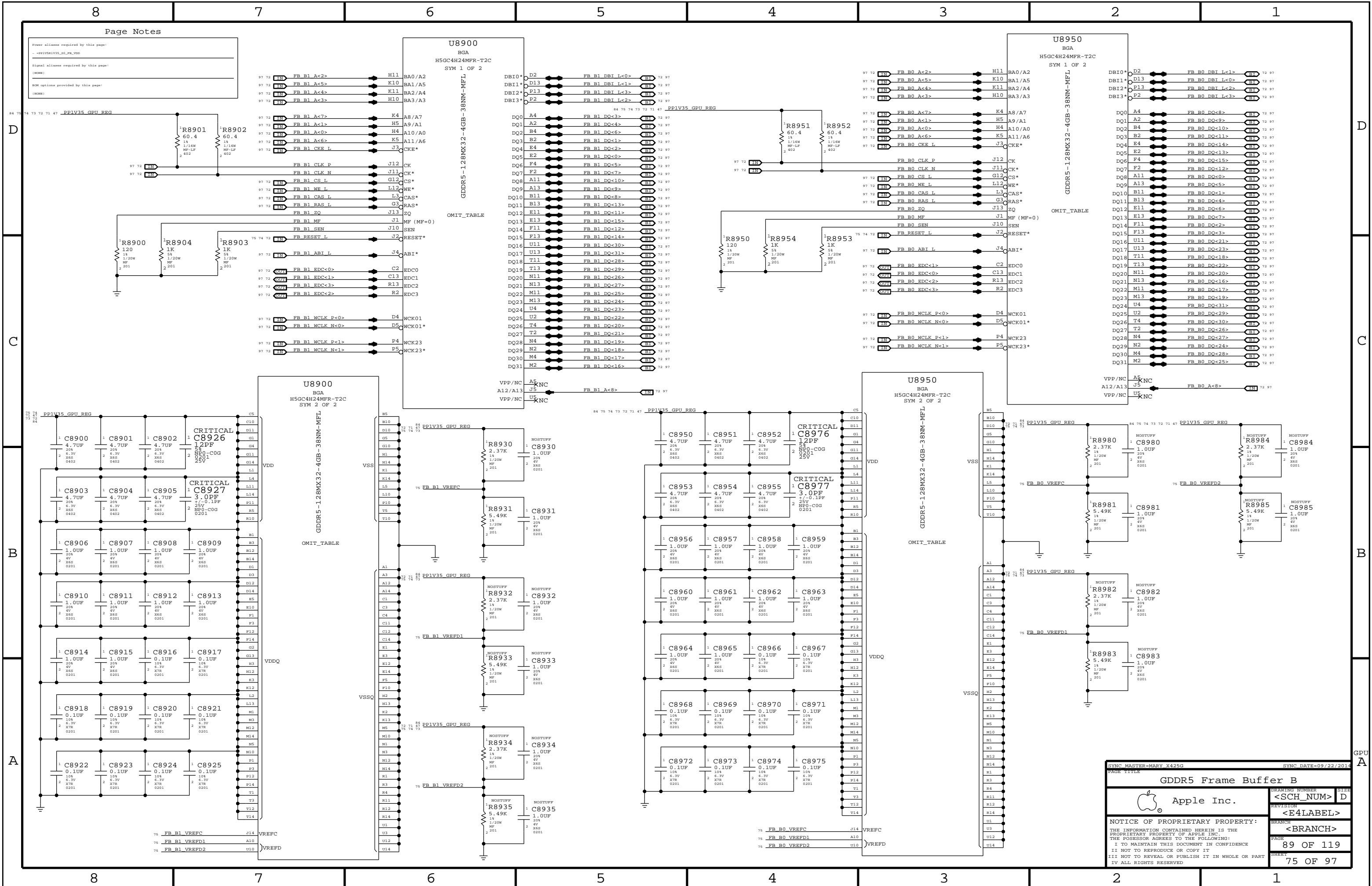
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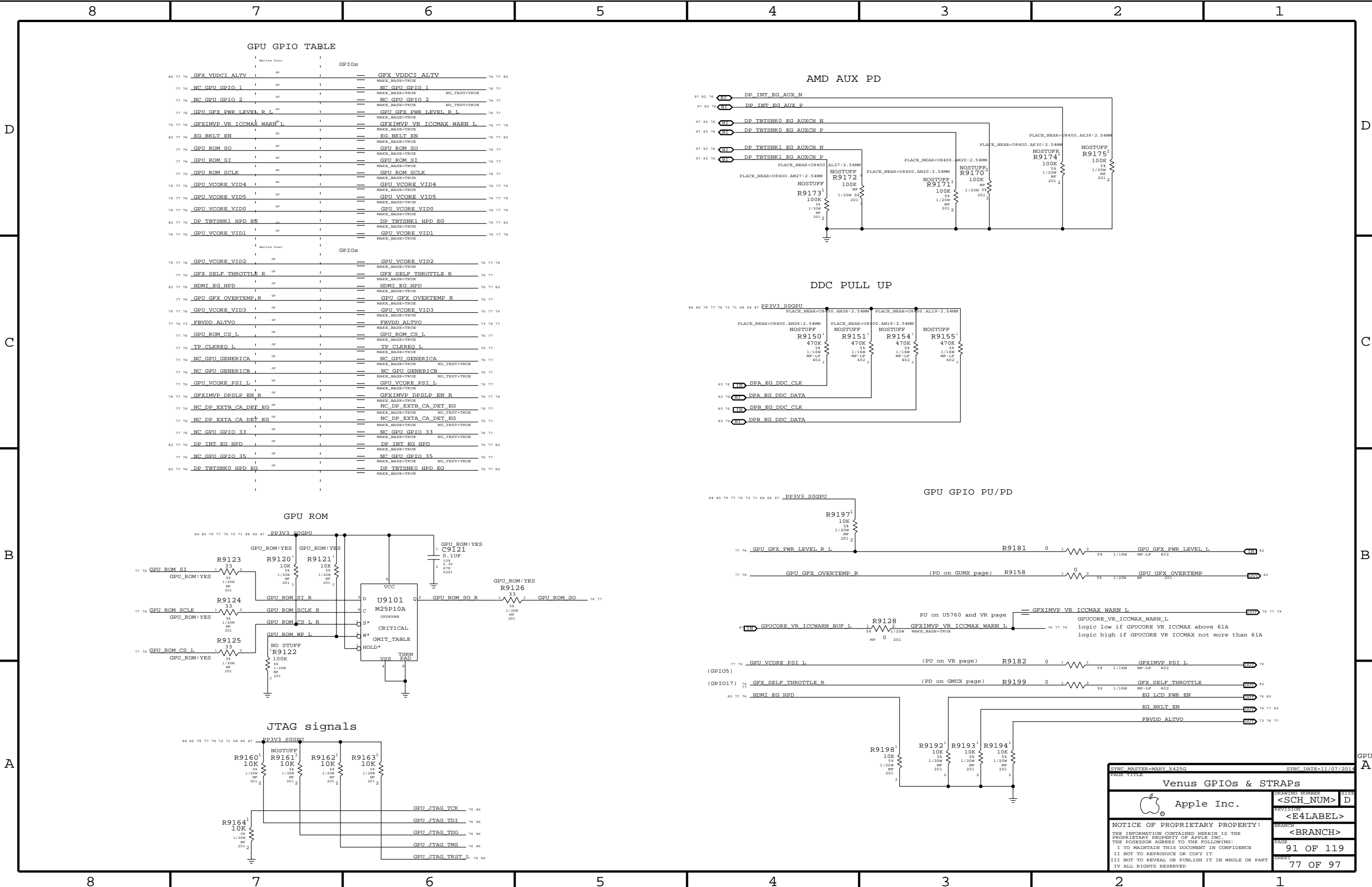
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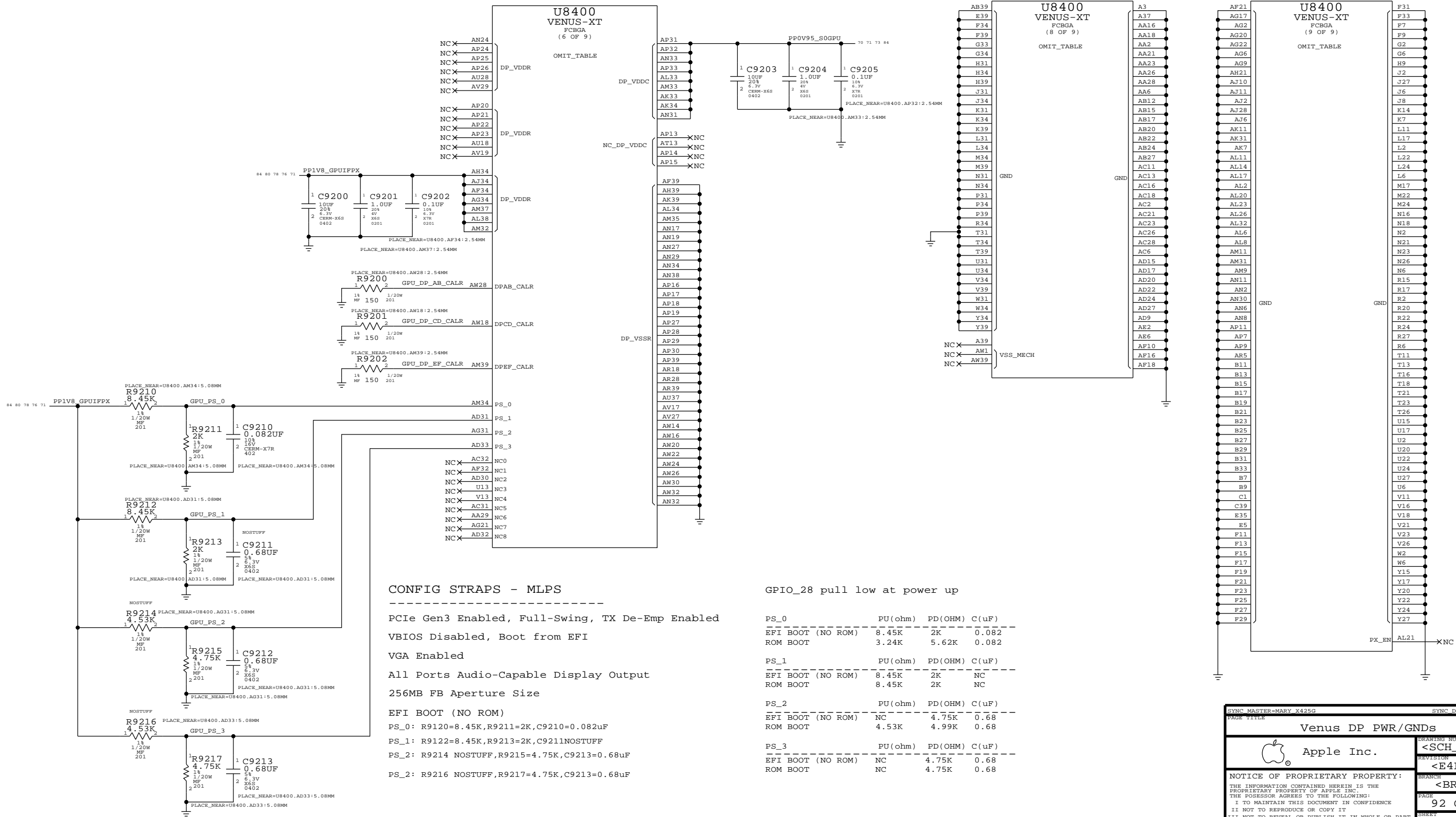




Power aliases required by this page:
- +PP1V8_GPU_PFX
- +PP1V8_GPU_CD
- +PP1V8_GPU_EF
- +PP1V8_GPU_AB
- +PP1V8_GPU_CD
- +PP1V8_GPU_EF

Signal aliases required by this page:
(NONE)

ROM options provided by this page:
(NONE)



SYNC MASTER=MARY X425G SYNC DATE=09/22/2014

PAGE TITLE

Venus DP PWR/GNDs

Apple Inc.

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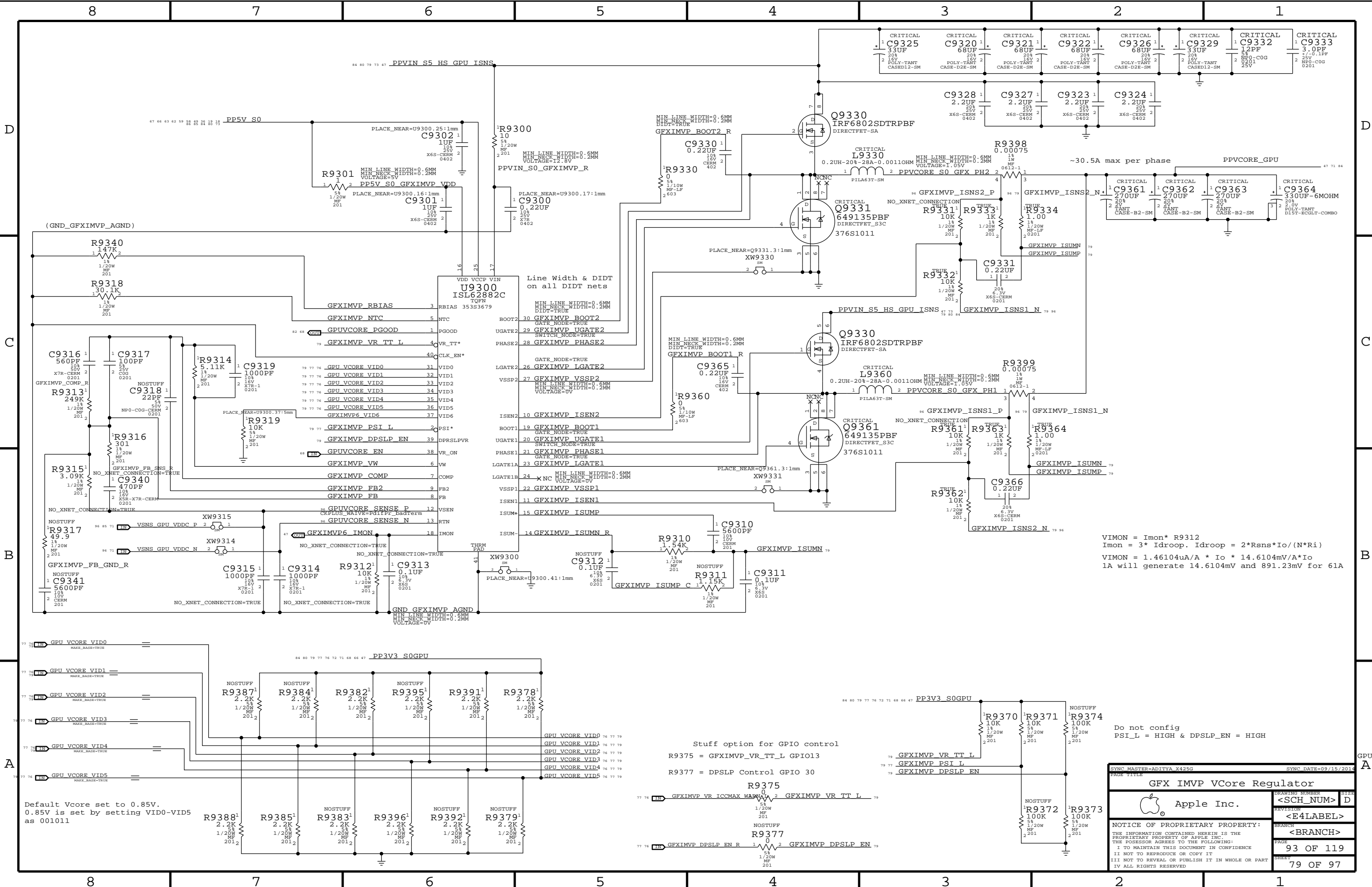
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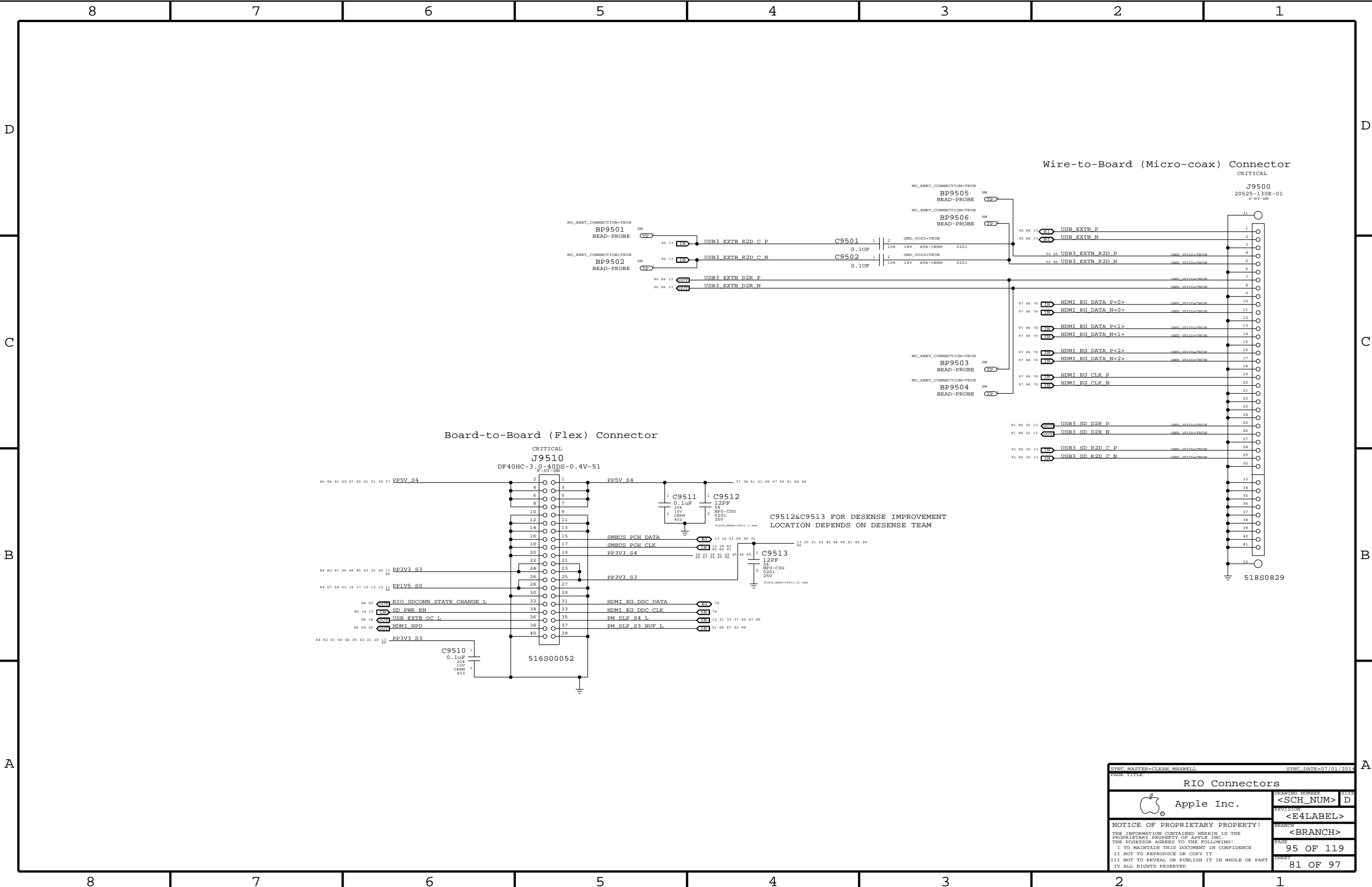


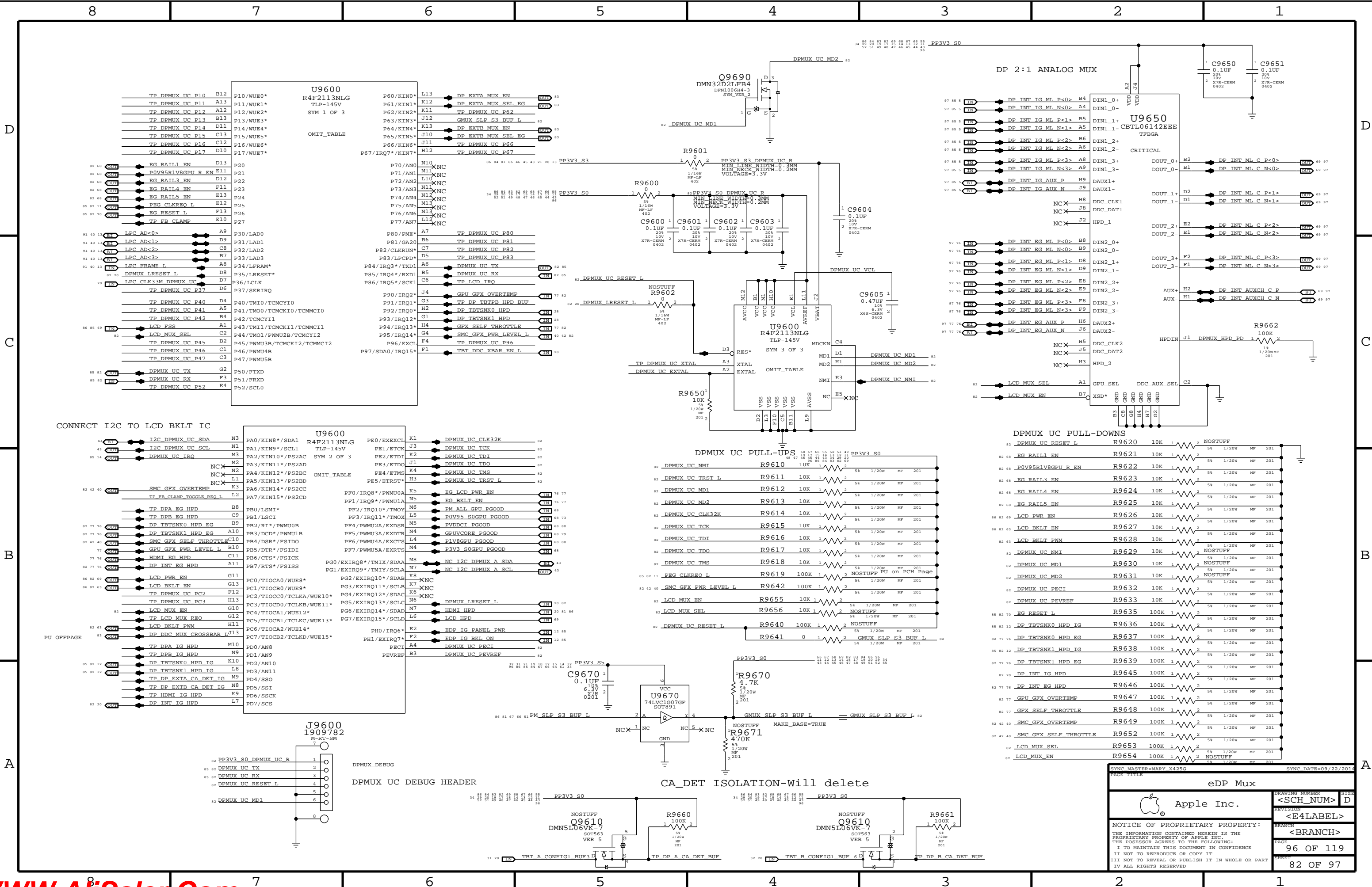
VIMON = Imon* R9312
Imon = 3* Idroop. Idroop = 2*Rsns*Io/(N*Ri)
VIMON = 1.46104uA/A * Io * 14.6104mV/A*Io
1A will generate 14.6104mV and 891.23mV for 61A

Do not config
PSI_L = HIGH & DPSLP_EN = HIGH

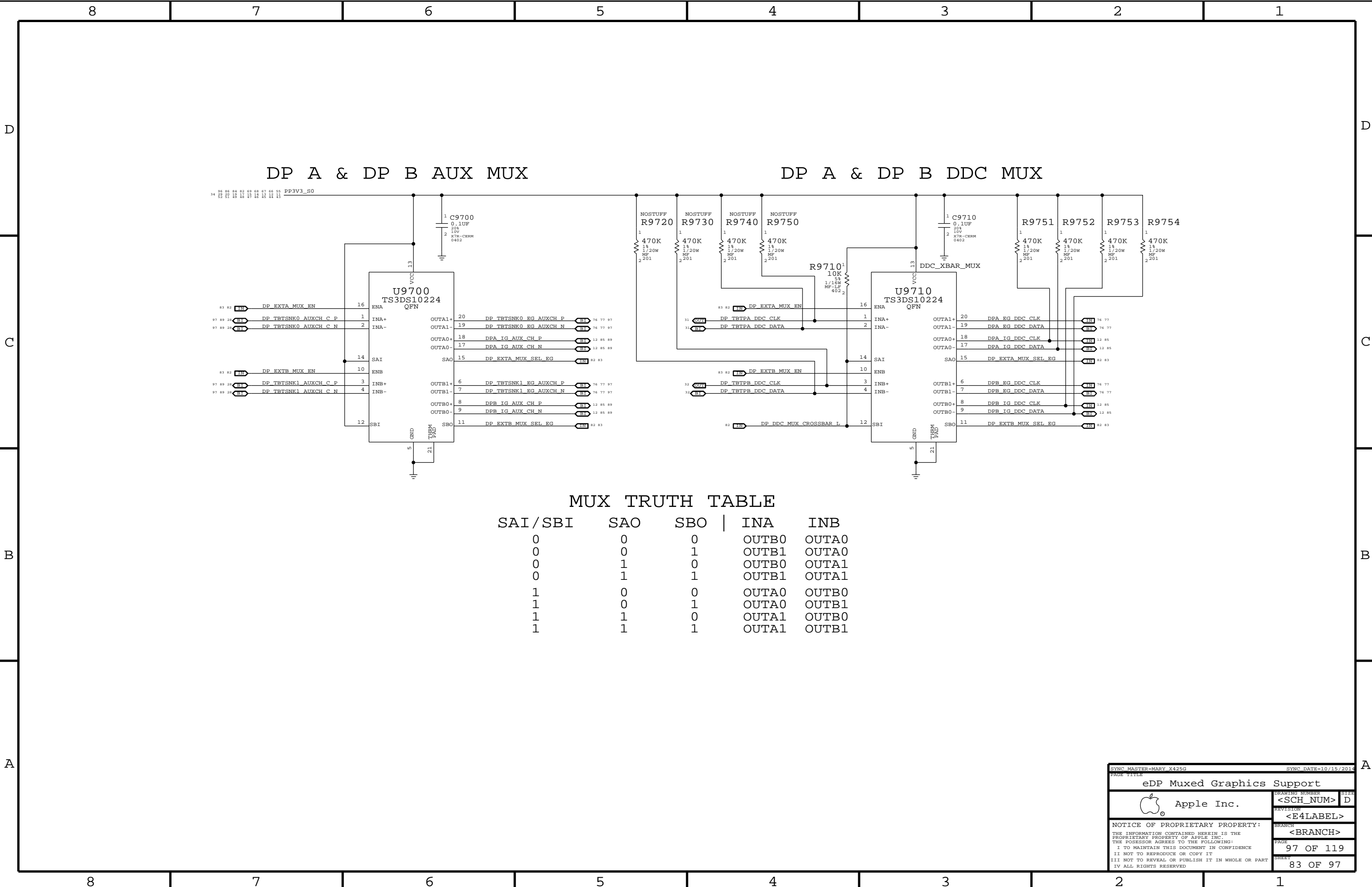
Stuff option for GPIO control
R9375 = GFXIMVP_VR_TT_L GPIO13
R9377 = DPSLP Control GPIO 30

SYNC MASTER=ADITYA X425G		SYNC DATE=09/15/2014	
PAGE TITLE		DRAWING NUMBER	
GFX IMVP VCore Regulator		<SCH_NUM>	
Apple Inc.		SIZE	
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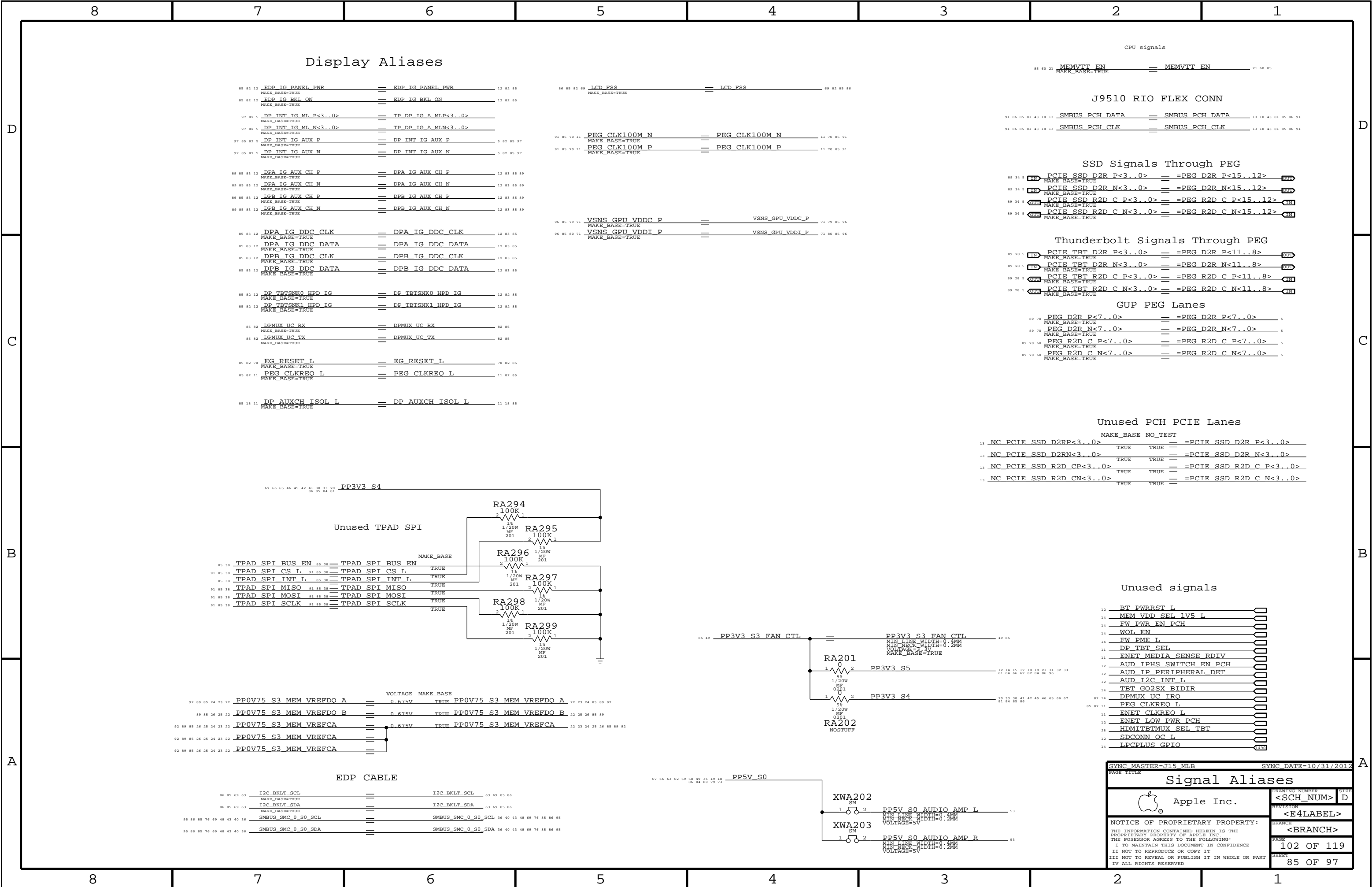


Apple Inc.		eDP Mux	
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MUX TRUTH TABLE

SAI/SBI	SAO	SBO	INA	INB
0	0	0	OUTB0	OUTA0
0	0	1	OUTB1	OUTA0
0	1	0	OUTB0	OUTA1
0	1	1	OUTB1	OUTA1
1	0	0	OUTA0	OUTB0
1	0	1	OUTA0	OUTB1
1	1	0	OUTA1	OUTB0
1	1	1	OUTA1	OUTB1



Functional Test Points

FUNC_TEST J3501 - airport		
TRUE	AP CLKREQ O L	33
TRUE	AP RESET CONN L	33
TRUE	PCIE AP D2R PI N	91
TRUE	PCIE AP D2R PI P	91
TRUE	PCIE AP R2D N	33 91
TRUE	PCIE AP R2D P	33 91
TRUE	PCIE CLK100M AP CONN N	33 91
TRUE	PCIE CLK100M AP CONN P	33 91
TRUE	PCIE WAKE L	12 33 35 91
TRUE	PP3V3 S3RS4 BT F	33
TRUE	PP3V3 WLAN	33 41
TRUE	USB BT CONN N	33 90
TRUE	USB BT CONN P	33 90
TRUE	WIFI EVENT L	33 40 41
TRUE	GND	4X

J4002 - Camera		
TRUE	MIPI CLK CONN N	36 94
TRUE	MIPI CLK CONN P	36 94
TRUE	CAM SENSOR WAKE L CONN	36
TRUE	MIPI DATA CONN N	36 94
TRUE	MIPI DATA CONN P	36 94
TRUE	SMBUS SMC 0 S0 SDA	36 40 43 48 69 76 85 86 95
TRUE	SMBUS SMC 0 S0 SCL	36 40 43 48 69 76 85 86 95
TRUE	I2C CAM SCK	35 36
TRUE	I2C CAM SDA	35 36
TRUE	PP5V S3RS0 ALSCAM F	36
TRUE	GND	

J9500 - rio coax		
TRUE	HDMI EG CLK N	76 81 97
TRUE	HDMI EG CLK P	76 81 97
TRUE	HDMI EG DATA N<0>	76 81 97
TRUE	HDMI EG DATA N<1>	76 81 97
TRUE	HDMI EG DATA N<2>	76 81 97
TRUE	HDMI EG DATA P<0>	76 81 97
TRUE	HDMI EG DATA P<1>	76 81 97
TRUE	HDMI EG DATA P<2>	76 81 97

TRUE	USB3 SD D2R N	13 20 81 91
TRUE	USB3 SD D2R P	13 20 81 91
TRUE	USB3 SD R2D C N	13 20 81 91
TRUE	USB3 SD R2D C P	13 20 81 91
TRUE	USB3 EXTB D2R N	13 81 90
TRUE	USB3 EXTB D2R P	13 81 90
TRUE	USB3 EXTB R2D N	81 90
TRUE	USB3 EXTB R2D P	81 90
TRUE	USB EXTB N	13 81 90
TRUE	USB EXTB P	13 81 90
TRUE	GND	19X

J9510 - rio flex		
TRUE	SD PWR EN	13 18 81
TRUE	HDMI DDC CLK	
TRUE	HDMI DDC DATA	
TRUE	HDMI HPD	20 81 82
TRUE	SMBUS PCH CLK	13 18 43 81 85 91
TRUE	SMBUS PCH DATA	13 18 43 81 85 91
TRUE	PM SLP S3 BUF L	51 66 67 81 82
TRUE	PM SLP S4 L	12 21 33 37 40 67 81
TRUE	PP3V3 S3	3X13 20 21 43 45 46 66 81 82
TRUE	PP3V3 S4	20 33 38 41 42 45 46 65 66 67
TRUE	PP5V S4	5X20 38 51 61 66 67 69 81 84
TRUE	RIO SDCONN STATE CHANGE L	86
TRUE	USB EXTB OC L	18 81
TRUE	GND	10X

J5150 - hall effect		
TRUE	PP3V42 G3H	19 34 37 38 40 41 42 43 50 56
TRUE	SMC LID R	42
TRUE	GND	

J6050 - left fan		
TRUE	FAN LT PWM	49
TRUE	FAN LT TACH	49
TRUE	PP5V S0	3X18 19 36 49 58 59 62 63 66
TRUE	GND	5X

J6060 - right fan		
TRUE	FAN RT PWM	49
TRUE	FAN RT TACH	49
TRUE	PP5V S0	3X18 19 36 49 58 59 62 63 66
TRUE	GND	5X

FUNC_TEST J6100 - spi		
TRUE	PP3V42 G3H	19 34 37 38 40 41 42 43 50 56
TRUE	SMC RESET L	40 41 50 57
TRUE	SMC TCK	40 41 50
TRUE	SMC TMS	40 41 50
TRUE	SPIROM USE MLB	14 50
TRUE	GND	2X

J4801 - ipd flex		
TRUE	USB TPAD N	13 38 90
TRUE	USB TPAD P	13 38 90
TRUE	IOXP2 INT L	38
TRUE	I2C IOXP SCL	38
TRUE	I2C IOXP SDA	38
TRUE	SMC PME S4 WAKE L	13 38 40 42
TRUE	TPAD ACTUATOR THRMTTRIP L	38 65
TRUE	TPAD VBUS EN	38 67
TRUE	SMBUS SMC 2 S3 SCL	38 40 43 95
TRUE	SMBUS SMC 2 S3 SDA	38 40 43 95
TRUE	SMC LID	38 40 41 42
TRUE	SMC ACTUATOR EN L	38 40
TRUE	PPVIN S4 TPAD	4X38 45 84
TRUE	GND ACTUATOR	4X38
TRUE	PP3V3 S4	20 33 38 41 42 45 46 65 66 67
TRUE	PP5V S4	81 84 85 86
TRUE	GND	2X

J4813 - keyboard		
TRUE	PP3V3 S4	20 33 38 41 42 45 46 65 66 67
TRUE	PP3V42 G3H	19 34 37 38 40 41 42 43 50 56
TRUE	WS CONTROL KBD	38
TRUE	WS KBD1	38
TRUE	WS KBD10	38
TRUE	WS KBD11	38
TRUE	WS KBD12	38
TRUE	WS KBD13	38
TRUE	WS KBD14	38
TRUE	WS KBD15 CAP	38
TRUE	WS KBD16 NUM	38
TRUE	WS KBD17	38
TRUE	WS KBD18	38
TRUE	WS KBD19	38
TRUE	WS KBD20	38
TRUE	WS KBD21	38
TRUE	WS KBD22	38
TRUE	WS KBD23	38
TRUE	WS KBD3	38
TRUE	WS KBD4	38
TRUE	WS KBD5	38
TRUE	WS KBD6	38
TRUE	WS KBD7	38
TRUE	WS KBD8	38
TRUE	WS KBD9	38
TRUE	WS KBD ONOFF L	38
TRUE	WS LEFT OPTION KBD	38
TRUE	WS LEFT SHIFT KBD	38
TRUE	GND	2X

J4915 - kbd bklt		
TRUE	KBDBKLT RETURN1	2X39 63
TRUE	KBDBKLT RETURN2	2X39 63
TRUE	PPVOUT S0 KBDBKLT	39 63
TRUE	GND	4X

J6601 - mic		
TRUE	DMIC CLK3	52 55
TRUE	PP3V3 S0	66 67 68 69 82 83 84 86 96
TRUE	DMIC SDA2	55
TRUE	DMIC SDA3	52 55
TRUE	GND	

J6602 - L speaker		
TRUE	SPKRCONN L ID	52 55
TRUE	SPKRCONN L OUT N	53 55 96
TRUE	SPKRCONN L OUT P	53 55 96
TRUE	SPKRCONN SL OUT N	53 55 96
TRUE	SPKRCONN SL OUT P	53 55 96
TRUE	GND	

J6603 - R speaker		
TRUE	SPKRCONN R ID	52 55
TRUE	SPKRCONN R OUT N	53 55 96
TRUE	SPKRCONN R OUT P	53 55 96
TRUE	SPKRCONN SR OUT N	53 55 96
TRUE	SPKRCONN SR OUT P	53 55 96
TRUE	GND	

J7000 - DC PWR		
TRUE	ADAPTER SENSE	56
TRUE	PP20V DCIN FUSE	2X56
TRUE	GND	2X

J7050 - battery		
TRUE	PPVBAT G3H CONN	8X56 57
TRUE	SMBUS SMC 5 G3 SCL	40 43 56 57 95
TRUE	SMBUS SMC 5 G3 SDA	40 43 56 57 95
TRUE	SYS DETECT L	56
TRUE	GND	8X

J8300 - eDP		
TRUE	DP INT AUX N	69 97
TRUE	DP INT AUX P	69 97
TRUE	DP INT ML N<0>	69 97
TRUE	DP INT ML N<1>	69 97
TRUE	DP INT ML N<2>	69 97
TRUE	DP INT ML N<3>	69 97
TRUE	DP INT ML P<0>	69 97
TRUE	DP INT ML P<1>	69 97
TRUE	DP INT ML P<2>	69 97
TRUE	DP INT ML P<3>	69 97
TRUE	LCD FSS	69 82 85
TRUE	LCD HPD CONN	69
TRUE	LCD BKLT PWM R	63 69
TRUE	SMBUS SMC 0 S0 SDA	36 40 43 48 69 76 85 86 95
TRUE	SMBUS SMC 0 S0 SCL	36 40 43 48 69 76 85 86 95
TRUE	I2C BKLT SDA	63 69 85
TRUE	I2C BKLT SCL	63 69 85
TRUE	PP5VR3V3 SW LCD	3X69
TRUE	PPVOUT S0 LCDBKLT	63 69
TRUE	GND	16X

Power Rails		
TRUE	PM SLP S3 L	12 21 40 67
TRUE	PPVTT S0 DDR	21 27 60 84
TRUE	PP3V3 S0	66 67 68 69 82 83 84 86 96
TRUE	PP3V3 S3	12 13 14 15 17 18 20 28 34
TRUE	PP3V3 S5	12 20 21 43 45 46 66 81 82 84
TRUE	PP3V3 S5 AVREF SMC	22 23 24 25 27 28 29 30 31 32 33
TRUE	PP3V42 G3H	40 41
TRUE	PP5V S0	19 34 37 38 40 41 42 43 50 56
TRUE	PP5V S3	19 34 37 38 40 41 42 43 50 56
TRUE	PP5V S5	21 36 60 66 67 84
TRUE	PPBUS G3H	61 66 84
TRUE	PPDCIN G3H	30 44 47 56 57 63 65 84
TRUE	PPVCC S0 CPU	56 57 84
TRUE	PPVTDDR S3	6 8 10 45 59 84
TRUE	PP3V3 S0SW SSD	40 84
TRUE	PP1V5 S0	34 45 84
TRUE	PP1V35 S3	21 45 60 66 84

FUNC_TEST XDP		
TRUE	XDP CPU TCK	6 18 89
TRUE	XDP PCH TCK	11 18
TRUE	XDP CPU TDI	6 18 89
TRUE	XDP CPU TDO	6 18 89
TRUE	XDP CPUPCH TRST L	6 18 89
TRUE	XDP CPU TMS	6 18 89
TRUE	XDP PCH TMS	11 18
TRUE	XDP PCH TDI	11 18
TRUE	XDP PCH TDO	11 18
TRUE	XDP CPU FREQ L	6 18 89
TRUE	XDP CPU PRDY L	6 18 89
TRUE	PM RSMRST L	12 67 91
TRUE	PM PCH PWROK	12 19 91
TRUE	PM SYSRST L	12 19 40 91
TRUE	CPU CFG<3>	6 18 89
TRUE	PP1V05 S0	10 14 15 17 18 41 62 67 84
TRUE	GND	2X GND

FUNC_TEST Power Sequence		
TRUE	SMC ONOFF L	38 40 41
TRUE	PM DSW PWROK	12 40 91
TRUE	ALL SYS PWROK	18 19 40 58 67
TRUE	PM PCH SYS PWROK	12 18 19 40 91
TRUE	PLT RESET L	12 18 20 21
TRUE	LCD PWR EN	69 82
TRUE	LCD BKLT EN	63 82

FUNC_TEST GPU_VENUS JTAG		
TRUE	GPU JTAG TCK	76 77
TRUE	GPU JTAG TDI	76 77
TRUE	GPU JTAG TDO	76 77
TRUE	GPU JTAG TMS	76 77
TRUE	GPU JTAG TRST L	76 77
TRUE	GPU PWROK	76 77

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PAGE TITLE			
Functional Test Points		DRAWING NUMBER	SIZE
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		<BRANCH>	
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8	7	6	5	4	3	2	1
NC NO_TESTS							
D	PCH		Thunderbolt		PLACEABLE BEAD-PROBES FOR TBT		
	NO_TEST MAKE_BASE		NO_TEST MAKE_BASE				
	87 13	NC USB3 SPARE D2RN	==	TRUE	TRUE	NC USB3 SPARE D2RN	13 87
	87 13	NC USB3 SPARE D2RP	==	TRUE	TRUE	NC USB3 SPARE D2RP	13 87
	87 13	NC USB3 SPARE R2D CN	==	TRUE	TRUE	NC USB3 SPARE R2D CN	13 87
	87 13	NC USB3 SPARE R2D CP	==	TRUE	TRUE	NC USB3 SPARE R2D CP	13 87
	90 87 13	NC USB3 EXTC D2RN	==	TRUE	TRUE	NC USB3 EXTC D2RN	13 87 90
	90 87 13	NC USB3 EXTC D2RP	==	TRUE	TRUE	NC USB3 EXTC D2RP	13 87 90
	90 87 13	NC USB3 EXTC R2D CN	==	TRUE	TRUE	NC USB3 EXTC R2D CN	13 87 90
	90 87 13	NC USB3 EXTC R2D CP	==	TRUE	TRUE	NC USB3 EXTC R2D CP	13 87 90
	90 87 13	NC USB3 EXTD D2RN	==	TRUE	TRUE	NC USB3 EXTD D2RN	13 87 90
	90 87 13	NC USB3 EXTD D2RP	==	TRUE	TRUE	NC USB3 EXTD D2RP	13 87 90
	90 87 13	NC USB3 EXTD R2D CN	==	TRUE	TRUE	NC USB3 EXTD R2D CN	13 87 90
	90 87 13	NC USB3 EXTD R2D CP	==	TRUE	TRUE	NC USB3 EXTD R2D CP	13 87 90
	87	NC PCIE ENET D2RN	==	TRUE	TRUE	NC PCIE ENET D2RN	87
	87	NC PCIE ENET D2RP	==	TRUE	TRUE	NC PCIE ENET D2RP	87
	87	NC PCIE ENET R2D CN	==	TRUE	TRUE	NC PCIE ENET R2D CN	87
	87	NC PCIE ENET R2D CP	==	TRUE	TRUE	NC PCIE ENET R2D CP	87
	87 12	NC DP IG D AUXCHN	==	TRUE	TRUE	NC DP IG D AUXCHN	12 87
	87 12	NC DP IG D AUXCHP	==	TRUE	TRUE	NC DP IG D AUXCHP	12 87
C	90 87 11	NC SATA A D2RN	==	TRUE	TRUE	NC SATA A D2RN	11 87 90
	90 87 11	NC SATA A D2RP	==	TRUE	TRUE	NC SATA A D2RP	11 87 90
	90 87 11	NC SATA A R2D CN	==	TRUE	TRUE	NC SATA A R2D CN	11 87 90
	90 87 11	NC SATA A R2D CP	==	TRUE	TRUE	NC SATA A R2D CP	11 87 90
	90 87 11	NC SATA B D2RN	==	TRUE	TRUE	NC SATA B D2RN	11 87 90
	90 87 11	NC SATA B D2RP	==	TRUE	TRUE	NC SATA B D2RP	11 87 90
	90 87 11	NC SATA B R2D CN	==	TRUE	TRUE	NC SATA B R2D CN	11 87 90
	90 87 11	NC SATA B R2D CP	==	TRUE	TRUE	NC SATA B R2D CP	11 87 90
	90 87 11	NC SATA ODD D2RN	==	TRUE	TRUE	NC SATA ODD D2RN	11 87 90
	90 87 11	NC SATA ODD D2RP	==	TRUE	TRUE	NC SATA ODD D2RP	11 87 90
	90 87 11	NC SATA ODD R2D CN	==	TRUE	TRUE	NC SATA ODD R2D CN	11 87 90
	90 87 11	NC SATA ODD R2D CP	==	TRUE	TRUE	NC SATA ODD R2D CP	11 87 90
	90 87 11	NC SATA D D2RN	==	TRUE	TRUE	NC SATA D D2RN	11 87 90
	90 87 11	NC SATA D D2RP	==	TRUE	TRUE	NC SATA D D2RP	11 87 90
	90 87 11	NC SATA D R2D CN	==	TRUE	TRUE	NC SATA D R2D CN	11 87 90
	90 87 11	NC SATA D R2D CP	==	TRUE	TRUE	NC SATA D R2D CP	11 87 90
	90 87 11	NC SATA F D2RN	==	TRUE	TRUE	NC SATA F D2RN	11 87 90
	90 87 11	NC SATA F D2RP	==	TRUE	TRUE	NC SATA F D2RP	11 87 90
	90 87 11	NC SATA F R2D CN	==	TRUE	TRUE	NC SATA F R2D CN	11 87 90
	90 87 11	NC SATA F R2D CP	==	TRUE	TRUE	NC SATA F R2D CP	11 87 90
B	90 87 13	NC USB EXTCN	==	TRUE	TRUE	NC USB EXTCN	13 87 90
	90 87 13	NC USB EXTCP	==	TRUE	TRUE	NC USB EXTCP	13 87 90
	90 87 13	NC USB SDN	==	TRUE	TRUE	NC USB SDN	13 87 90
	90 87 13	NC USB SDP	==	TRUE	TRUE	NC USB SDP	13 87 90
	87 13	NC USB WLANN	==	TRUE	TRUE	NC USB WLANN	87
	87 13	NC USB WLANP	==	TRUE	TRUE	NC USB WLANP	87
	90 87 13	NC USB 6N	==	TRUE	TRUE	NC USB 6N	13 87 90
	90 87 13	NC USB 6P	==	TRUE	TRUE	NC USB 6P	13 87 90
	90 87 13	NC USB 7N	==				

```

93 31 28 TBT A D2R P<1> 1 TPD SM BEAD-PROBE BPA531 NO_XNET_CONNECTION=TRUE
93 31 28 TBT A D2R N<1> 1 TPD SM BEAD-PROBE BPA532 NO_XNET_CONNECTION=TRUE

```

87	12	<u>NC DP IG D AUXCHN</u>	<u>—</u>	<u>TRUE</u>	<u>TRUE</u>	<u>NC DP IG D AUXCHN</u>	12	87
87	12	<u>NC DP IG D AUXCHP</u>	<u>—</u>	<u>TRUE</u>	<u>TRUE</u>	<u>NC DP IG D AUXCHP</u>	12	87

NC	PCIE	CLK100M	PE5N	---	TRUE	TRUE	NC	PCIE	CLK100M	PE5N	13	8
NC	PCIE	CLK100M	PE5P	---	TRUE	TRUE	NC	PCIE	CLK100M	PE5P	13	8
NC	PCIE	CLK100M	ENETSDN	---	TRUE	TRUE	NC	PCIE	CLK100M	ENETSDN	13	8
NC	PCIE	CLK100M	ENETSDP	---	TRUE	TRUE	NC	PCIE	CLK100M	ENETSDP	13	8
NC	PCIE	CLK100M	ENETN	---	TRUE	TRUE	NC	PCIE	CLK100M	ENETN	13	8
NC	PCIE	CLK100M	ENETP	---	TRUE	TRUE	NC	PCIE	CLK100M	ENETP	13	8
NC	PCIE	CLK100M	PEGBN	---	TRUE	TRUE	NC	PCIE	CLK100M	PEGBN	13	8
NC	PCIE	CLK100M	PEGBP	---	TRUE	TRUE	NC	PCIE	CLK100M	PEGBP	13	8
NC	PCIE	CLK100M	SWN	---	TRUE	TRUE	NC	PCIE	CLK100M	SWN	13	8
NC	PCIE	CLK100M	SWP	---	TRUE	TRUE	NC	PCIE	CLK100M	SWP	13	8

NC	PCH	GPIO64	CLKOUTFLEX0	=	TRUE	TRUE	NC	PCH	GPIO64	CLKOUTFLEX0	11
NC	PCH	GPIO65	CLKOUTFLEX1	=	TRUE	TRUE	NC	PCH	GPIO65	CLKOUTFLEX1	11
NC	PCH	GPIO66	CLKOUTFLEX2	=	TRUE	TRUE	NC	PCH	GPIO66	CLKOUTFLEX2	11
NC	PCH	GPIO67	CLKOUTFLEX3	=	TRUE	TRUE	NC	PCH	GPIO67	CLKOUTFLEX3	11

NC USB 4N	==	TRUE	TRUE	NC USB 4N	13 87
NC USB 4P	==	TRUE	TRUE	NC USB 4P	13 87

TP_DVPCNTL1_M<1..0>	TRUE	TRUE	NC_DVPCNTL1_M<1..0>	76
TP_DVPCNTL2..0>	TRUE	TRUE	NC_DVPCNTL2..0>	76
NC_DVPCCLK	TRUE	TRUE	NC_DVPCCLK	76
NC_DPVDATA<23..6>	TRUE	TRUE	NC_DPVDATA<23..6>	76
NC_FB_B0_A<9>	TRUE	TRUE	NC_FB_B0_A<9>	77
NC_FB_B1_A<9>	TRUE	TRUE	NC_FB_B1_A<9>	77
NC_FB_A0_A<9>	TRUE	TRUE	NC_FB_A0_A<9>	77
NC_FB_A1_A<9>	TRUE	TRUE	NC_FB_A1_A<9>	77

TRUE	PCIE TBT R2D P<3...0>	28 89
TRUE	PCIE TBT R2D N<3...0>	28 89
TRUE	PCIE TBT D2R C P<3...0>	28 89
TRUE	PCIE TBT D2R C N<3...0>	28 89

Fig 9	TRUE	DMI S2N P<3..1>	5	12	89
Fig 9	TRUE	DMI S2N N<3..1>	5	12	89
Fig 9	TRUE	DMI N2S P<3..1>	5	12	89
Fig 9	TRUE	DMI N2S N<3..1>	5	12	89

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87 12 NC EDP IG BKL PWM      — TRUE      TRUE      NC EDP IG BKL PWM      12 87

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90	87	NC USB SMCN	==	TRUE	TRUE	NC USB SMCN	87	90
90	87	NC USB SMCN	==	TRUE	TRUE	NC USB SMCN	87	90

X425G BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM	NO_TYPE, BGA, P65BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2, ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules


Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3, ISL4, ISL9, ISL10	0.053 MM	?
1x_DIELECTRIC	ISL2, ISL5, ISL6, ISL7, ISL8, ISL11	0.101 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?	CPU_VID	*	0.457 MM	?
CPU_COMP	*	20 MIL	?	CPU_VREF	*	12 MIL	?
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	*	=3X_DIELECTRIC	?	DMI_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DMI_TXRX	*	=6X_DIELECTRIC	?	DMI_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICKLK2N2S	*	=6X_DIELECTRIC	?	DMICKLK2N2S	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICKLK2S2N	*	=3X_DIELECTRIC	?	DMICKLK2S2N	TOP,BOTTOM	=6X_DIELECTRIC	?
DMICKLK2OTHER	*	=4X_DIELECTRIC	?	DMICKLK2OTHER	TOP,BOTTOM	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_*	=SAME	*	DMI_2SAME
DMI_N2S	DMI_S2N	*	DMI_TXRX
DMI_S2N	DMI_N2S	*	DMI_TXRX
CLK_DMI	DMI_N2S	*	DMICKLK2N2S
CLK_DMI	DMI_S2N	*	DMICKLK2S2N
CLK_DMI	*	*	DMICKLK2OTHER

PEG - SSD & TBT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	*	=3X_DIELECTRIC	?	PEG_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PEG_TXRX	*	=6X_DIELECTRIC	?	PEG_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PEG_2OTHER	*	=4X_DIELECTRIC	?	PEG_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG_2CLK	*	=7X_DIELECTRIC	?	PEG_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG3_2SAME	*	=4X_DIELECTRIC	?	PEG3_2SAME	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG3_TXRX	*	=8X_DIELECTRIC	?	PEG3_TXRX	TOP,BOTTOM	=12X_DIELECTRIC	?
PEG3_2OTHER	*	=5X_DIELECTRIC	?	PEG3_2OTHER	TOP,BOTTOM	=8X_DIELECTRIC	?
PEG3_2CLK	*	=8X_DIELECTRIC	?	PEG3_2CLK	TOP,BOTTOM	=12X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_*	=SAME	*	PEG_2SAME	PEG3_*	=SAME	*	PEG3_2SAME
PEG_R2D	PEG_D2R	*	PEG_TXRX	PEG3_R2D	PEG3_D2R	*	PEG3_TXRX
PEG_*	*	*	PEG_2OTHER	PEG3_*	*	*	PEG3_2OTHER
PEG_*	CLK_*	*	PEG_2CLK	PEG3_*	CLK_*	*	PEG3_2CLK

DIGITAL VIDEO SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3X_DIELECTRIC	?	DP_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DP_2OTHER	*	=4X_DIELECTRIC	?	DP_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
HDMICKLK_2CLK	*	=7X_DIELECTRIC	?	HDMICKLK_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
HDMICKLK_2DP	*	=6X_DIELECTRIC	?	HDMICKLK_2DP	TOP,BOTTOM	=6X_DIELECTRIC	?
HDMICKLK_2OTHER	*	=7X_DIELECTRIC	?	HDMICKLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	*	*	DP_2OTHER
HDMI_CLK	CLK_*	*	HDMICKLK_2CLK
HDMI_CLK	DISPLAYPORT	*	HDMICKLK_2DP
HDMI_CLK	*	*	HDMICKLK_2OTHER

DisplayPort/TMDs intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.

DisplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.

SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N P<3:0>	5 12 87
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N N<3:0>	5 12 87
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S P<3:0>	5 12 87
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S N<3:0>	5 12 87
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	5 12
FDI_CSYNCR	CPU_50S	CPU_AGTL	FDI_CSYNCR	5 12
CLK_DMI	CPU_85D	CLK_DMI	DMI_CLK100M CPU P	6 11
CLK_DMI	CPU_85D	CLK_DMI	DMI_CLK100M CPU N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M DPLLREF N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M DPLLREF P	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M DPLLSS N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M DPLLSS P	6 11
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU EDP RCOMP	5
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU PEG RCOMP	5
CPU_CFG	CPU_45S	CPU_ITP	CPU CFG<19..0>	6 18 86
XDP_CLK_BCH	CLK_PCIE_85D	CLK_PCIE	NC ITPXDP CLK100MP	11 87
XDP_CLK_BCH	CLK_PCIE_85D	CLK_PCIE	NC ITPXDP CLK100MN	11 87
XDP_TDI	CPU_45S	CPU_ITP	XDP CPU TDI	6 18 86
XDP_TDO	CPU_45S	CPU_ITP	XDP CPU TDO	6 18 86
XDP_TMS	CPU_45S	CPU_ITP	XDP CPU TMS	6 18 86
XDP_TCK	CPU_45S	CPU_ITP	XDP CPU TCK	6 18 86
XDP_TRST_L	CPU_45S	CPU_ITP	XDP CRUPCH TRST_L	6 18 86
XDP_BPM	CPU_45S	CPU_ITP	XDP BPM L<3..0>	6 18
XDP_BPM_L	CPU_45S	CPU_ITP	XDP BPM L<7..4>	6 18
XDP_DBRESET_L	CPU_45S	CPU_ITP	XDP DBRESET_L	6 18 19
XDP_PRDY_L	CPU_45S	CPU_ITP	XDP CPU PRDY_L	6 18 86
XDP_PREQ_L	CPU_45S	CPU_ITP	XDP CPU PREQ_L	6 18 86
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU CATERR_L	6 40
CPU_PECI	CPU_45S	CPU_VID	CPU Peci	6 14 41
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU PROCHOT_L	6 40 41 58
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU PWRGD	6 14 18
PM_THRMTRIP_L	CPU_45S	CPU_AGTL	PM THRMTRIP_L	6 14 41
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM MEM_PWRGD	6 12 21
PM_SYNC	CPU_45S	CPU_AGTL	PM SYNC	6 12
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU SM_RCOMP<2..0>	6
CPU_VIDSOUT	CPU_45S	CPU_VID	CPU VIDSOUT	8 58
CPU_VIDCLK	CPU_45S	CPU_VID	CPU VIDCLK	8 58
CPU_VIDALERT_L	CPU_45S	CPU_VID	CPU VIDALERT_L	8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	9 58
CPU_MEM_VREF	MEM_12MIL		CPU DIMMA VREFDQ	7 22
CPU_MEM_VREF	MEM_12MIL		CPU DIMMB VREFDQ	7 22
CPU_MEM_VREF	MEM_PWR		PPOV75 S3 MEM VREFDQ A	22 23 24 85 92
CPU_MEM_VREF	MEM_PWR		PPOV75 S3 MEM VREFDQ B	22 25 26 85
CPU_MEM_VREF	MEM_PWR		PPOV75 S3 MEM VREFCA	22 23 24 25 26 85 89 92
CPU_MEM_VREF	MEM_PWR		PPOV75 S3 MEM VREFCA	22 23 24 25 26 85 89 92
PCIE_D2R_GPU	PEG_80D	PEG3_D2R	PEG D2R C P<7..0>	68 70
PCIE_D2R_GPU	PEG_80D	PEG3_D2R	PEG D2R C N<7..0>	68 70
PCIE_D2R_GPU	PEG_80D	PEG3_D2R	PEG D2R P<7..0>	70 85
PCIE_D2R_GPU	PEG_80D	PEG3_D2R	PEG D2R N<7..0>	70 85
PCIE_R2D_GPU	PEG_80D	PEG3_R2D	PEG R2D C P<7..0>	68 70 85
PCIE_R2D_GPU	PEG_80D	PEG3_R2D	PEG R2D C N<7..0>	68 70 85
PCIE_R2D_GPU	PEG_80D	PEG3_R2D	PEG R2D P<7..0>	70
PCIE_R2D_GPU	PEG_80D	PEG3_R2D	PEG R2D N<7..0>	70
PCIE_D2R_SSD	CPU_85D	PEG3_D2R	PCIE SSD D2R P<3..0>	5 34 85
PCIE_D2R_SSD	CPU_85D	PEG3_D2R	PCIE SSD D2R N<3..0>	5 34 85
PCIE_R2D_SSD	CPU_85D	PEG3_R2D	PCIE SSD R2D C P<3..0>	5 34 85
PCIE_R2D_SSD	CPU_85D	PEG3_R2D	PCIE SSD R2D C N<3..0>	5 34 85
PCIE_R2D_SSD	CPU_85D	PEG3_R2D	PCIE SSD R2D P<3..0>	34
PCIE_R2D_SSD	CPU_85D	PEG3_R2D	PCIE SSD R2D N<3..0>	34
PCIE_TBT_D2R	CPU_85D	PEG_D2R	PCIE TBT D2R P<3..0>	5 28 85
PCIE_TBT_D2R	CPU_85D	PEG_D2R	PCIE TBT D2R N<3..0>	5 28 85
PCIE_TBT_D2R	CPU_85D	PEG_D2R	PCIE TBT D2R C P<3..0>	28 87
PCIE_TBT_D2R	CPU_85D	PEG_D2R	PCIE TBT D2R C N<3..0>	28 87
PCIE_TBT_R2D	CPU_85D	PEG_R2D	PCIE TBT R2D P<3..0>	28 87
PCIE_TBT_R2D	CPU_85D	PEG_R2D	PCIE TBT R2D N<3..0>	28 87
PCIE_TBT_R2D	CPU_85D	PEG_R2D	PCIE TBT R2D C P<3..0>	5 28 85
PCIE_TBT_R2D	CPU_85D	PEG_R2D	PCIE TBT R2D C N<3..0>	5 28 85

DP AUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DP_IG_AUX	DP_85D	DISPLAYPORT	DPA_IG_AUX_CH_P	12 83 85
DP_IG_AUX	DP_85D	DISPLAYPORT	DPA_IG_AUX_CH_N	12 83 85
DP_IG_AUX	DP_85D	DISPLAYPORT	DPB_IG_AUX_CH_P	12 83 85
DP_IG_AUX	DP_85D	DISPLAYPORT	DPB_IG_AUX_CH_N	12 83 85

DP / HDMI NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP TBTSNK0 ML C P<3..0>	28 76 97
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP TBTSNK0 ML C N<3..0>	28 76 97
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP TBTSNK0 ML P<3..0>	28 97
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP TBTSNK0 ML N<3..0>	28 97
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP TBTSNK1 ML C P<3..0>	28 76 97
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP TBTSNK1 ML C N<3..0>	28 76 97
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP TBTSNK1 ML P<3..0>	28 97
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP TBTSNK1 ML N<3..0>	28 97
TBTSNK_AUXCH	DP_85D		DP TBTSNK0 AUXCH P	28 97
TBTSNK_AUXCH	DP_85D		DP TBTSNK0 AUXCH N	28 97
TBTSNK_AUXCH	DP_85D		DP TBTSNK0 AUXCH C P	28 83 97
TBTSNK_AUXCH	DP_85D		DP TBTSNK0 AUXCH C N	28 83 97
TBTSNK_AUXCH	DP_85D		DP TBTSNK1 AUXCH P	28 97
TBTSNK_AUXCH	DP_85D		DP TBTSNK1 AUXCH N	28 97
TBTSNK_AUXCH	DP_85D		DP TBTSNK1 AUXCH C P	28 83 97
TBTSNK_AUXCH	DP_85D		DP TBTSNK1 AUXCH C N	28 83 97

SYNC MASTER=CLEAN X305 PEG SYNC DATE=02/18/2014

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?
SATA_RCOMP	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
SATA_RCOMP	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	=SAME	*	SATA_2SAME
SATA_R2D	SATA_D2R	*	SATA_TXRX
SATA_*	*	*	SATA_2OTHER

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?
WT_WAKE	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?
WT_WAKE	TOP,BOTTOM	=6X_DIELECTRIC	?

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	=SAME	*	USB3_2SAME
USB3_R2D	USB3_D2R	*	USB3_TXRX
USB3_*	*	*	USB3_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4X_DIELECTRIC	?
CLK_25M	*	=5X_DIELECTRIC	?


NOTE: 25MHz system clocks very sensitive to noise.
NOTE: Latest Intel DG calls out 50ohms SE for sys clocks

PCH Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
<div></div>	SATA_R5D	SATA_R2D	NC SATA A R2D CP 11 87
<div></div>	SATA_85D	SATA_R2D	NC SATA A R2D CN 11 87
<div></div>	SATA_85D	SATA_D2R	NC SATA A D2RP 11 87
<div></div>	SATA_85D	SATA_D2R	NC SATA A D2RN 11 87
<div></div>	SATA_85D	SATA_R2D	NC SATA B R2D CP 11 87
<div></div>	SATA_85D	SATA_R2D	NC SATA B R2D CN 11 87
<div></div>	SATA_85D	SATA_D2R	NC SATA B D2RP 11 87
<div></div>	SATA_85D	SATA_D2R	NC SATA B D2RN 11 87
<div></div>			
<div></div>	PCH_SATA_RCOMP	SATA_45SE	SATA_RCOMP PCH SATA RCOMP 11
<div></div>	USB_EXTN	USB_85D	USB USB_EXTN_P 13 37
<div></div>	USB_EXTN	USB_85D	USB USB_EXTN_N 13 37
<div></div>	USB_EXTN	USB_85D	USB USB_EXTN_MUXED_P 37
<div></div>	USB_EXTN	USB_85D	USB USB_EXTN_MUXED_N 37
<div></div>	USB_EXTN	USB_85D	USB USB_LT1_P 37
<div></div>	USB_EXTN	USB_85D	USB USB_LT1_N 37
<div></div>			
<div></div>	USB_NC	USB_85D	NC USB_EXTCP 13 87
<div></div>	USB_NC	USB_85D	NC USB_EXTCN 13 87
<div></div>	USB_NC	USB_85D	NC USB_SDP 13 87
<div></div>	USB_NC	USB_85D	NC USB_SDN 13 87
<div></div>	CPU_45S	CPU_ITP	SMC_DEBUGPRT_RX_L 37 40 41
<div></div>	CPU_45S	CPU_ITP	SMC_DEBUGPRT_TX_L 37 40 41
<div></div>	USB_SMC	USB_85D	NC USB_SMCP 87
<div></div>	USB_SMC	USB_85D	NC USB_SMCN 87
<div></div>			
<div></div>	USB_NC	USB_85D	NC USB_6P 13 87
<div></div>	USB_NC	USB_85D	NC USB_6N 13 87
<div></div>	USB_NC	USB_85D	NC USB_7P 13 87
<div></div>	USB_NC	USB_85D	NC USB_7N 13 87
<div></div>	USB_EXTB	USB_85D	USB USB_EXTB_P 13 81 86
<div></div>	USB_EXTB	USB_85D	USB USB_EXTB_N 13 81 86
<div></div>	USB_NC	USB_85D	NC USB_EXTRDP 13 87
<div></div>	USB_NC	USB_85D	NC USB_EXTRDN 13 87
<div></div>	USB_BT	USB_85D	USB BT_P 13 33
<div></div>	USB_BT	USB_85D	USB BT_N 13 33
<div></div>	USB_BT	USB_85D	USB BT_CONN_P 33 86
<div></div>	USB_BT	USB_85D	USB BT_CONN_N 33 86
<div></div>	USB_NC	USB_85D	NC USB_IRP 13 87
<div></div>	USB_NC	USB_85D	NC USB_IRN 13 87
<div></div>	USB_TPAD	USB_85D	USB USB_TPAD_P 13 38 86
<div></div>	USB_TPAD	USB_85D	USB USB_TPAD_N 13 38 86
<div></div>	USB_TPAD	USB_85D	USB USB_TPAD_R_P
<div></div>	USB_TPAD	USB_85D	USB USB_TPAD_R_N
<div></div>	PCH_USB_RBIAS	PCH_USB_RBIAS	USB USB_RBIAS 13
<div></div>			
<div></div>	USB3_EXTN_RX	USB_85D	USB3 USB3_EXTN_D2R_P 13 37
<div></div>	USB3_EXTN_RX	USB_85D	USB3 USB3_EXTN_D2R_N 13 37
<div></div>	USB_85D	USB3_D2R	USB3 USB3_EXTN_D2R_C_P
<div></div>	USB_85D	USB3_D2R	USB3 USB3_EXTN_D2R_C_N
<div></div>	USB3_EXTN_TX	USB_85D	USB3 USB3_EXTN_R2D_P 37
<div></div>	USB3_EXTN_TX	USB_85D	USB3 USB3_EXTN_R2D_N 37
<div></div>	USB_85D	USB3_R2D	USB3 USB3_EXTN_R2D_C_P 13 37
<div></div>	USB_85D	USB3_R2D	USB3 USB3_EXTN_R2D_C_N 13 37
<div></div>	USB3_EXTB_RX	USB_85D	USB3 USB3_EXTB_D2R_P 13 81 86
<div></div>	USB3_EXTB_RX	USB_85D	USB3 USB3_EXTB_D2R_N 13 81 86
<div></div>	USB_85D	USB3_D2R	USB3 USB3_EXTB_D2R_C_P
<div></div>	USB_85D	USB3_D2R	USB3 USB3_EXTB_D2R_C_N
<div></div>	USB3_EXTB_TX	USB_85D	USB3 USB3_EXTB_R2D_P 81 86
<div></div>	USB3_EXTB_TX	USB_85D	USB3 USB3_EXTB_R2D_N 81 86
<div></div>	USB_85D	USB3_R2D	USB3 USB3_EXTB_R2D_C_P 13 81
<div></div>	USB_85D	USB3_R2D	USB3 USB3_EXTB_R2D_C_N 13 81
<div></div>	NC_USB3	USB_85D	NC USB3_EXTC_D2RP 13 87
<div></div>	NC_USB3	USB_85D	NC USB3_EXTC_D2RN 13 87
<div></div>	USB_85D	USB3_R2D	NC USB3_EXTC_R2D_CP 13 87
<div></div>	USB_85D	USB3_R2D	NC USB3_EXTC_R2D_CN 13 87
<div></div>	NC_USB3	USB_85D	NC USB3_EXTD_D2RP 13 87
<div></div>	NC_USB3	USB_85D	NC USB3_EXTD_D2RN 13 87
<div></div>	USB_85D	USB3_R2D	NC USB3_EXTD_R2D_CP 13 87
<div></div>	USB_85D	USB3_R2D	NC USB3_EXTD_R2D_CN 13 87

Clock Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
<div></div>	SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW SYSCLK_CLK32K_RTC 11 19
<div></div>	SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M SYSCLK_CLK25M_SB 11 19
<div></div>	SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M SYSCLK_CLK25M_CAMERA 11 19
<div></div>	SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M SYSCLK_CLK25M_TBT 19 28
<div></div>		CLK_25M_45S	CLK_25M SYSCLK_CLK25M_TBT_R 28

SYNC MASTER=SIDLE J45		SYNC DATE=12/10/2012	
PAGE TITLE			
PCH Constraints 1			
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTRL	*	=2x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CTRL2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Double checked with Doc#486985 Chief River SFF Platform DG: Memory Down
SOURCE: Need to re-confirm CRW DG for memory down (Intel not yet provided)

Memory to Power Spacing


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
	PHYSICAL	SPACING
MEM_A_CLK0	MEM_72D	MEM_CLK
MEM_A_CLK0	MEM_72D	MEM_CLK
MEM_A_CLK1	MEM_72D	MEM_CLK
MEM_A_CLK1	MEM_72D	MEM_CLK
MEM_A_CNTRL0	MEM_40S	MEM_CTRL
MEM_A_CNTRL1	MEM_40S	MEM_CTRL
MEM_A_CNTRL0	MEM_40S	MEM_CTRL
MEM_A_CNTRL1	MEM_40S	MEM_CTRL
MEM_A_CNTRL0	MEM_40S	MEM_CTRL
MEM_A_CNTRL1	MEM_40S	MEM_CTRL
MEM_A_CNTRL0	MEM_40S	MEM_CTRL
MEM_A_CNTRL1	MEM_40S	MEM_CTRL
MEM_A_CMD	MEM_40S	MEM_CMD
MEM_A_CMD	MEM_40S	MEM_CMD
MEM_A_CMD	MEM_40S	MEM_CMD
MEM_A_CMD	MEM_40S	MEM_CMD
MEM_A_CMD	MEM_40S	MEM_CMD
MEM_A_DATA_0	MEM_45S	MEM_A_DATA_0
MEM_A_DATA_1	MEM_45S	MEM_A_DATA_1
MEM_A_DATA_2	MEM_45S	MEM_A_DATA_2
MEM_A_DATA_3	MEM_45S	MEM_A_DATA_3
MEM_A_DATA_4	MEM_45S	MEM_A_DATA_4
MEM_A_DATA_5	MEM_45S	MEM_A_DATA_5
MEM_A_DATA_6	MEM_45S	MEM_A_DATA_6
MEM_A_DATA_7	MEM_45S	MEM_A_DATA_7
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7
MEM_B_CLK0	MEM_72D	MEM_CLK
MEM_B_CLK0	MEM_72D	MEM_CLK
MEM_B_CLK1	MEM_72D	MEM_CLK
MEM_B_CLK1	MEM_72D	MEM_CLK
MEM_B_CNTRL0	MEM_40S	MEM_CTRL
MEM_B_CNTRL1	MEM_40S	MEM_CTRL
MEM_B_CNTRL0	MEM_40S	MEM_CTRL
MEM_B_CNTRL1	MEM_40S	MEM_CTRL
MEM_B_CNTRL0	MEM_40S	MEM_CTRL
MEM_B_CNTRL1	MEM_40S	MEM_CTRL
MEM_B_CMD	MEM_40S	MEM_CMD
MEM_B_CMD	MEM_40S	MEM_CMD
MEM_B_CMD	MEM_40S	MEM_CMD
MEM_B_CMD	MEM_40S	MEM_CMD
MEM_B_DATA_0	MEM_45S	MEM_B_DATA_0
MEM_B_DATA_1	MEM_45S	MEM_B_DATA_1
MEM_B_DATA_2	MEM_45S	MEM_B_DATA_2
MEM_B_DATA_3	MEM_45S	MEM_B_DATA_3
MEM_B_DATA_4	MEM_45S	MEM_B_DATA_4
MEM_B_DATA_5	MEM_45S	MEM_B_DATA_5
MEM_B_DATA_6	MEM_45S	MEM_B_DATA_6
MEM_B_DATA_7	MEM_45S	MEM_B_DATA_7
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7
		MEM_PWR
		MEM_PWR
		MEM_PWR

SYNC MASTER=SIDLE J45		SYNC DATE=12/10/2012	
PAGE TITLE			
Memory Constraints			
	Apple Inc.	DRAWING NUMBER	SIZE
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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

TBT_DP Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTD_P85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTD_P_2SAME	*	=3X_DIELECTRIC	?
TBTD_P_TXRX	*	=6X_DIELECTRIC	?
TBTD_P_2OTHER	*	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTD_P_*	=SAME	*	TBTD_P_2SAME
TBTD_P_R2D	TBTD_P_D2R	*	TBTD_P_TXRX
TBTD_P_*	*	*	TBTD_P_2OTHER

Thunderbolt/DP Net Properties


ELECTRICAL CONSTRAINT SET		NET_TYPE		
PHYSICAL		SPACING		
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT A R2D C P<1..0>	28 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT A R2D C N<1..0>	28 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT A R2D P<1..0>	31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT A R2D N<1..0>	31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPA ML C P<1>	28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPA ML C N<1>	28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPA ML P<1>	31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPA ML N<1>	31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP A LSX ML P<1>	31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP A LSX ML N<1>	31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML C P<3>	28 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML C N<3>	28 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML P<3>	31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML N<3>	31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT A D2R C P<0>	31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT A D2R C N<0>	31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT A D2R P<0>	28 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT A D2R N<0>	28 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R C P<1>	31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R C N<1>	31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R P<1>	28 31 8
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R N<1>	28 31 8
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R1 AUXDDC P	31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R1 AUXDDC N	31
TBT_A_AUXCH	DP_85D		DP TBTPA AUXCH C P	28 31
TBT_A_AUXCH	DP_85D		DP TBTPA AUXCH C N	28 31
TBT_A_AUXCH	DP_85D		DP TBTPA AUXCH P	31
TBT_A_AUXCH	DP_85D		DP TBTPA AUXCH N	31
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT B R2D C P<1..0>	28 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT B R2D C N<1..0>	28 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT B R2D P<1..0>	32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT B R2D N<1..0>	32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP TBTBP ML C P<1>	28 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP TBTBP ML C N<1>	28 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP TBTBP ML P<1>	32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP TBTBP ML N<1>	32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP B LSX ML P<1>	32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP B LSX ML N<1>	32
DP_TBTBP_ML	DP_85D	DISPLAYPORT	DP TBTBP ML C P<3>	28 32
DP_TBTBP_ML	DP_85D	DISPLAYPORT	DP TBTBP ML C N<3>	28 32
DP_TBTBP_ML	DP_85D	DISPLAYPORT	DP TBTBP ML P<3>	32
DP_TBTBP_ML	DP_85D	DISPLAYPORT	DP TBTBP ML N<3>	32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT B D2R C P<0>	32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT B D2R C N<0>	32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT B D2R P<0>	28 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT B D2R N<0>	28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R C P<1>	32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R C N<1>	32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R P<1>	28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R N<1>	28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R1 AUXDDC P	32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R1 AUXDDC N	32
TBT_B_AUXCH	DP_85D		DP TBTBP AUXCH C P	28 32
TBT_B_AUXCH	DP_85D		DP TBTBP AUXCH C N	28 32
TBT_B_AUXCH	DP_85D		DP TBTBP AUXCH P	32
TBT_B_AUXCH	DP_85D		DP TBTBP AUXCH N	32

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
0000	DP_85D	DISPLAYPORT	DP_TBTSRC ML C P<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC ML C N<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC AUXCH C P	
	DP_85D	DISPLAYPORT	DP_TBTSRC AUXCH C N	
0000	TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT SPI CLK
	TBT_SPI_M0GI	TBT_SPI_45S	TBT_SPI	TBT SPI MOSI
	TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT SPI MISO
	TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT SPI CS L

Only used on hosts supporting Thunderbolt video-in

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Thunderbolt Constraints			
 Apple Inc.		DRAWING NUMBER <SCH_NUM>	
		SIZE D	
		REVISION <E4LABEL>	
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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM CAM CLK P	35 36
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM CAM CLK N	35 36
S2_MEM_CNTRL	S2_MEM_45S	S2_MEM_CTRL	MEM CAM CKE	35 36
S2_MEM_CNTRL	S2_MEM_45S	S2_MEM_CTRL	MEM CAM CS L	35 36
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM CAM ODT	36
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM CAM CAS L	35 36
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM CAM RAS L	35 36
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM WE L	35 36
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM BA<0>	35 36
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM BA<1>	35 36
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM BA<2>	35 36
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM CAM DQS P<0>	35 36
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM CAM DQS N<0>	35 36
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM CAM DQS P<1>	35 36
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM CAM DQS N<1>	35 36
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM CAM DM<0>	35 36
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM CAM DM<1>	35 36
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM CAM A<14..0>	35 36
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM CAM DQ<7..0>	35 36
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM CAM DQ<15..8>	35 36
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA P	35 36
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA N	35 36
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA CONN P	36 86
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA CONN N	36 86
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK P	35 36
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK N	35 36
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK CONN P	36 86
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK CONN N	36 86
PPIV35_CAM		S2_MEM_PWR	PPIV35_CAM	35 36
PPOV675_CAM_VREF		S2_MEM_PWR	PPOV675_CAM_VREF	35 36
PPOV675_MEM_CAM_VREFCA		S2_MEM_PWR	PPOV675_MEM_CAM_VREFCA	36
PPOV675_MEM_CAM_VREFDQ		S2_MEM_PWR	PPOV675_MEM_CAM_VREFDQ	36

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D									D
C									C
B									B
A									A
	8	7	6	5	4	3	2	1	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_I701_508	*	+1:1_DIFFPAIR	+50_OHM_SE	+50_OHM_SE	+50_OHM_SE	+1:1_DIFFPAIR	+1:1_DIFFPAIR
THERM_I701_508	*	+1:1_DIFFPAIR	+50_OHM_SE	+50_OHM_SE	+50_OHM_SE	+1:1_DIFFPAIR	+1:1_DIFFPAIR
DIFFPAIR	*	+1:1_DIFFPAIR			+1:1_DIFFPAIR	+1:1_DIFFPAIR	+1:1_DIFFPAIR
AUDIODIFF	*	+1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
THERM_455_CPOVIDEN01	*	+1:1_DIFFPAIR	+45_OHM_SE	+45_OHM_SE	+45_OHM_SE	0.2 MM	0.2 MM
THERM_I701_455	*	+1:1_DIFFPAIR	+45_OHM_SE	+45_OHM_SE	+45_OHM_SE	+1:1_DIFFPAIR	+1:1_DIFFPAIR
SENSE_I701_455	*	+1:1_DIFFPAIR	+45_OHM_SE	+45_OHM_SE	+45_OHM_SE	+1:1_DIFFPAIR	+1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	-2K_DIELECTRIC	?
THERM	*	-2K_DIELECTRIC	?
AUDIO	*	-2K_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GSD	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GRID	*	GRID_P2004
CPU_VCCSENSE	GRID	*	GRID_P2004

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_F2M0
GND	PCIE_*	*	GND_F2M0
GND	SATA_*	*	GND_F2M0
USB	GND	*	GND_F2M0
CLK_PCIE	SB_POWER	*	PWR_F2M0
SB_POWER	SATA_*	*	PWR_F2M0
USB	SB_POWER	*	PWR_F2M0

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D	*			0.09 MM	10 MM		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
1TO1_DIFFPAIR	*	1:1_DIFFPAIR

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SEMI_GPUVR	*	Y	0.300 MM	0.200 MM	3.000 MM	0.400 MM	0.200 MM

AMD Net Properties


ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL		SPACING
1600	SENSE_DIFFPAIR	THERM 1701 45S	THERM	GPUFB CS P 47 73
1600	SENSE_DIFFPAIR	THERM 1701 45S	THERM	GPUFB CS N 47 73
1600	SENSE_DIFFPAIR	THERM 1701 45S	THERM	GPU TDIODE P 48 76
1600	SENSE_DIFFPAIR	THERM 1701 45S	THERM	GPU TDIODE N 48 76
1600	SENSE_DIFFPAIR	SENSE 1701 45S	SENSE	GPU VDDCISENSE P
1600	SENSE_DIFFPAIR	SENSE 1701 45S	SENSE	GPU VDDCISENSE N
1600	SENSE_DIFFPAIR	SENSE 1701 45S	SENSE	GPU VDDCI SENSE XW P 80
1600	SENSE_DIFFPAIR	SENSE 1701 45S	SENSE	GPU VDDCI SENSE XW N 80
1600	SENSE_DIFFPAIR	SENSE 1701 45S	SENSE	GPUVCORE SENSE P 79
1600	SENSE_DIFFPAIR	SENSE 1701 45S	SENSE	GPUVCORE SENSE N 79
1600	SENSE_DIFFPAIR	SENSE 1701 45S	SENSE	ISNS PP0V95 SOGPU R P 47
1600	SENSE_DIFFPAIR	SENSE 1701 45S	SENSE	ISNS PP0V95 SOGPU R N 47
1600	SENSE_DIFFPAIR	THERM 1701 45S	SENSE	VSNS_GPU_0V95_XW_P 73
1600	SENSE_DIFFPAIR	THERM 1701 45S	SENSE	VSNS_GPU_0V95_XW_N 73
1600	SENSE_DIFFPAIR	SENSE 1701 45S	SENSE	VDDCI50_CS_R_P 47
1600	SENSE_DIFFPAIR	SENSE 1701 45S	SENSE	VDDCI50_CS_R_N 47
1600	SENSE_DIFFPAIR	SENSE 1701 45S	SENSE	GPUFB CS R P 47
1600	SENSE_DIFFPAIR	SENSE 1701 45S	SENSE	GPUFB CS R N 47
1600	SENSE_DIFFPAIR	SENSE 1701 45S	SENSE	VSNS_GPU_VDDC_P 71
1600	SENSE_DIFFPAIR	SENSE 1701 45S	SENSE	VSNS_GPU_VDDC_N 71 79
1600	SENSE_DIFFPAIR	SENSE 1701 45S	SENSE	VSNS_GPU_VDDI_P 71 80
1600	SENSE_DIFFPAIR	SENSE 1701 45S	SENSE	VSNS_GPU_VDDI_N 71 80
1600	SENSE_DIFFPAIR	SENSE 1701 45S	SENSE	ISNS_1V8_GPU_R_P
1600	SENSE_DIFFPAIR	SENSE 1701 45S	SENSE	ISNS_1V8_GPU_R_N
1600	SENSE_DIFFPAIR	SENSE 1701 45S	SENSE	ISNS_1V8_GPU_P
1600	SENSE_DIFFPAIR	SENSE 1701 45S	SENSE	ISNS_1V8_GPU_N
1600	SENSE_DIFFPAIR	THERM 1701 45S	SENSE	VSNS_GPU_FB_XW_P 73
1600	SENSE_DIFFPAIR	THERM 1701 45S	SENSE	VSNS_GPU_FB_XW_N 73

X425G Specific Net Properties

ELECTRICAL_CONSTRAINT_SET		PHYSICAL	FEASIBLE	
E490	SENSE_DIEFFPAIR	THERM T101_45S	THERM	ISNS CPUDDR P
E491	SENSE_DIEFFPAIR	THERM T101_45S	THERM	ISNS CPUDDR N
E492	SENSE_DIEFFPAIR	THERM T101_45S	THERM	ISNS CPU DDR R P
E493	SENSE_DIEFFPAIR	THERM T101_45S	THERM	ISNS CPU DDR R N
E494	SENSE_DIEFFPAIR	THERM T101_45S	THERM	CPUTHMSNS D2 P
E495	SENSE_DIEFFPAIR	THERM T101_45S	THERM	CPUTHMSNS D2 N
E496	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS LCD PANEL P
E497	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS LCD PANEL N
E498	SENSE_DIEFFPAIR	THERM T101_45S	THERM	DDR3THMSNS D1 P
E499	SENSE_DIEFFPAIR	THERM T101_45S	THERM	DDR3THMSNS D1 N
E500	SENSE_DIEFFPAIR	THERM T101_45S	THERM	FINTHMSNS D P
E501	SENSE_DIEFFPAIR	THERM T101_45S	THERM	FINTHMSNS D N
E502	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS 1V35 MEM P
E503	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS 1V35 MEM N
E504	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS 1V35 MEM R P
E505	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS 1V35 MEM R N
E506	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS AIRPORT P
E507	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS AIRPORT N
E508	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS AIRPORT R P
E509	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS AIRPORT R N
E510	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS LCDBKLT P
E511	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS LCDBKLT N
E512	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS LCD PANEL P
E513	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS LCD PANEL N
E514	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS PCH R P
E515	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS PCH R N
E516	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS TPAD P
E517	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS TPAD N
E518	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS HS OTHER5V P
E519	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS HS OTHER5V N
E520	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS HS OTHER3V3 P
E521	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS HS OTHER3V3 N
E522	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS HS COMPUTING P
E523	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	ISNS HS COMPUTING N
E524	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	CPUVR ISNS P
E525	SENSE_DIEFFPAIR	SENSE T101_45S	SENSE	CPUVR ISNS N
E526	SENSE_DIEFFPAIR	THERM T101_45S	THERM	PLV05 GPU PEX IOVDD SNS P
E527	SENSE_DIEFFPAIR	THERM T101_45S	THERM	PLV05 GPU PEX IOVDD SNS N
E528	SENSE_DIEFFPAIR	THERM 45S CPUVRISNS1	THERM	DIFFERENTIAL_PAIR CPUVR ISNS1 CPUVR ISNS1 P
E529	SENSE_DIEFFPAIR	THERM 45S CPUVRISNS1	THERM	CPUVR ISNS1 CPUVR ISNS1 N
E530	SENSE_DIEFFPAIR	THERM 45S CPUVRISNS1	THERM	CPUVR ISNS2 CPUVR ISNS2 P
E531	SENSE_DIEFFPAIR	THERM 45S CPUVRISNS1	THERM	CPUVR ISNS2 CPUVR ISNS2 N
E532	SENSE_DIEFFPAIR	THERM 45S CPUVRISNS1	THERM	CPUVR ISNS3 CPUVR ISNS3 P
E533	SENSE_DIEFFPAIR	THERM 45S CPUVRISNS1	THERM	CPUVR ISNS3 CPUVR ISNS3 N
E534	SENSE_DIEFFPAIR	THERM T101_45S	THERM	CPUVR ISUM R P
E535	SENSE_DIEFFPAIR	THERM T101_45S	THERM	CPUVR ISUM R N
E536	SENSE_DIEFFPAIR	THERM T101_45S	THERM	GFXIMVP ISNS1 P
E537	SENSE_DIEFFPAIR	THERM T101_45S	THERM	GFXIMVP ISNS1 N
E538	SENSE_DIEFFPAIR	THERM T101_45S	THERM	GFXIMVP ISNS1 P
E539	SENSE_DIEFFPAIR	THERM T101_45S	THERM	GFXIMVP ISNS1 N
E540	AUDIO_DIEFFPAIR	AUDIODIFF	AUDIO	ISNS TBT N
E541	AUDIO_DIEFFPAIR	AUDIODIFF	AUDIO	ISNS TBT P
E542	AUDIO_DIEFFPAIR	AUDIODIFF	AUDIO	ISNS TBT R N
E543	AUDIO_DIEFFPAIR	AUDIODIFF	AUDIO	ISNS TBT R P
E544	SENSE_DIEFFPAIR	THERM T101_45S	THERM	ISNS SSD P
E545	SENSE_DIEFFPAIR	THERM T101_45S	THERM	ISNS SSD N
E546	SENSE_DIEFFPAIR	THERM T101_45S	THERM	ISNS SSD R P
E547	SENSE_DIEFFPAIR	THERM T101_45S	THERM	ISNS SSD R N
E548	SENSE_DIEFFPAIR	THERM T101_45S	THERM	PLV05S0 CS P
E549	SENSE_DIEFFPAIR	THERM T101_45S	THERM	PLV05S0 CS N
E550	SENSE_DIEFFPAIR	THERM T101_45S	THERM	DIFFERENTIAL_PAIR PLV05S0_SENSE PLV05S0_SENSE P
E551	SENSE_DIEFFPAIR	THERM T101_45S	THERM	PLV05S0_SENSE PLV05S0_SENSE N

X425G Specific Net Properties

[illegible]

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